JackHammer: Rowhammer and Cache Attacks on Heterogeneous FPGA-CPU Platforms

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October 2, 2020

UNIVERSITÄT ZU LÜBECK
INSTITUTE FOR IT SECURITY

Motivation

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Microsoft
Azure

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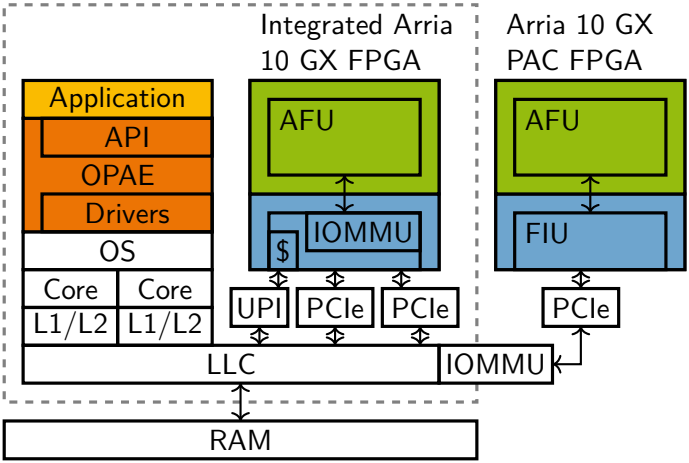

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Important Considerations

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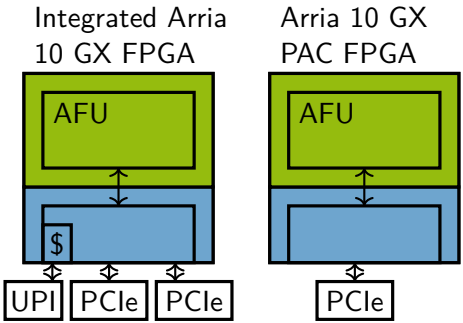
- Address spaces: physical, virtual, I/O virtual
- Pages (4 KB) and hugepages (2 MB)
- Which caches are/aren't modified by CPU/FPGA reads/writes/flushes

Background

Intel Acceleration Stack



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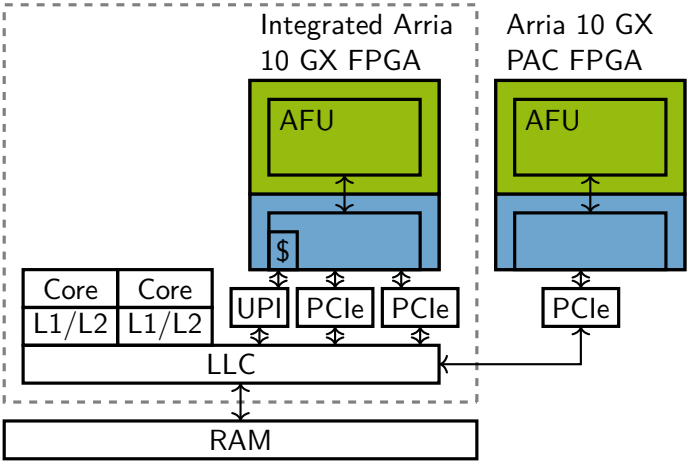

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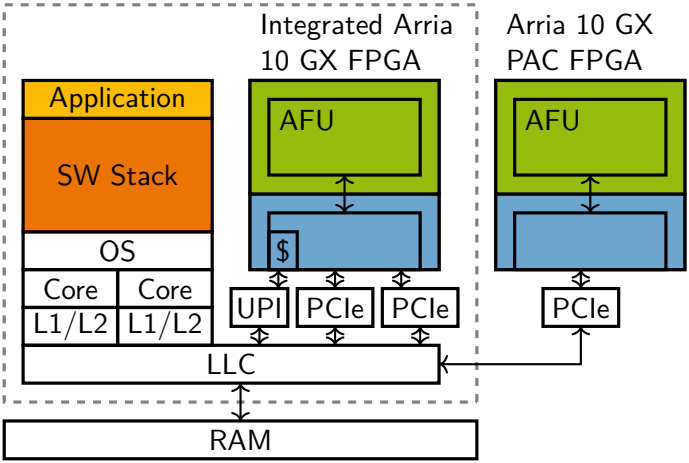

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Core Cache Interface Port

- MMIO
- DMA
  - Communication channels

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- MMIO
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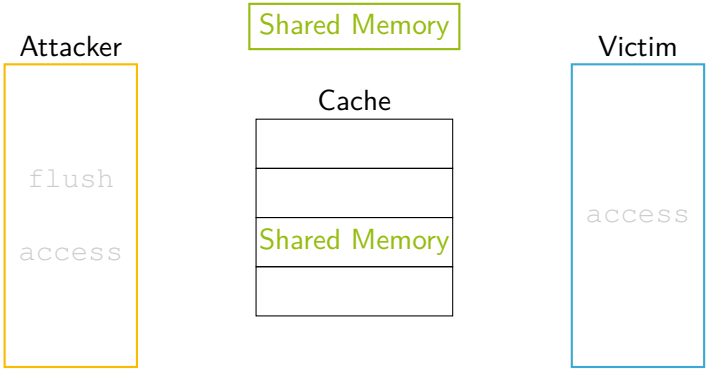
  - Communication channels
  - Physical addressing of (huge)pages
  - Caching hints

```
RdLine_I  WrLine_I
RdLine_S  WrLine_M
          WrPush_I
```

Cache Attacks

Background – Flush+Reload



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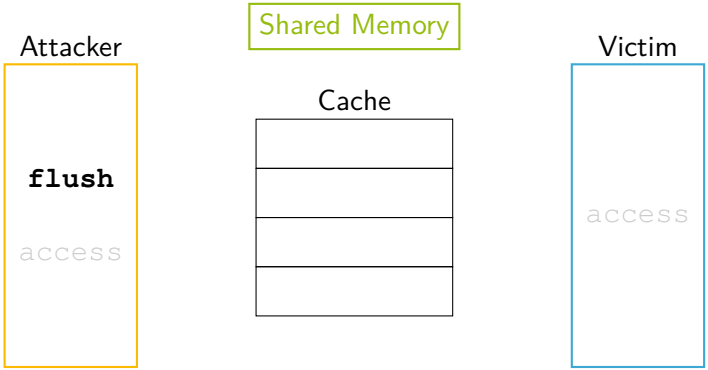

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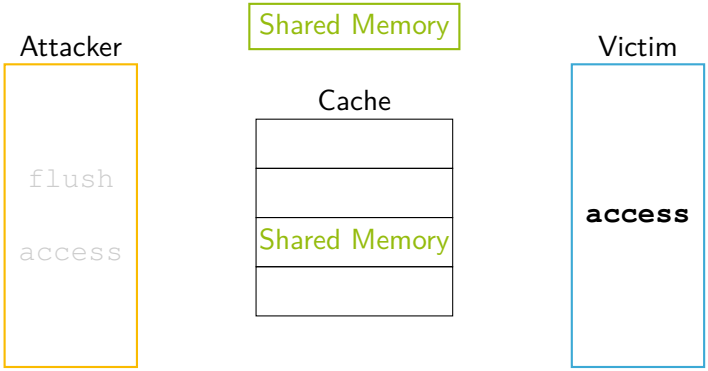

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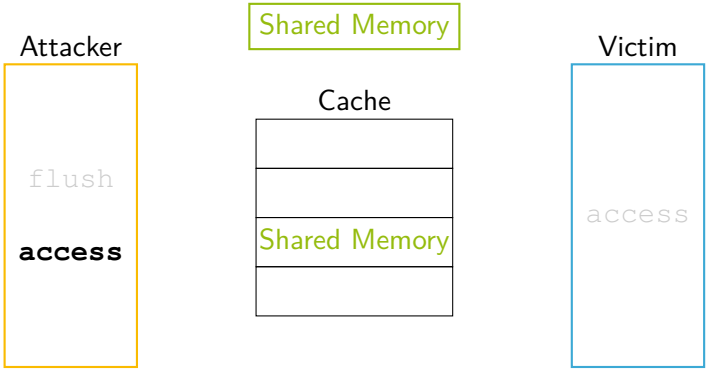

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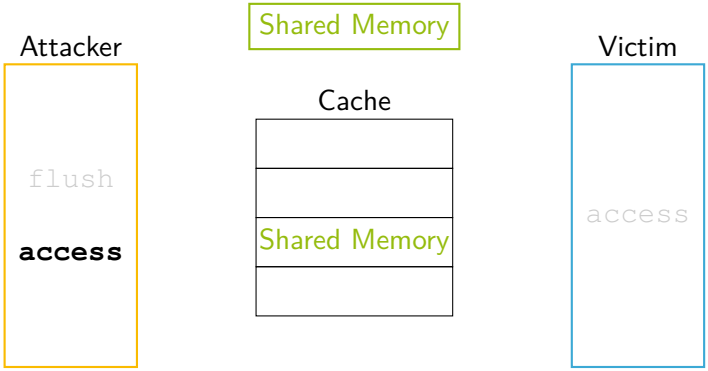

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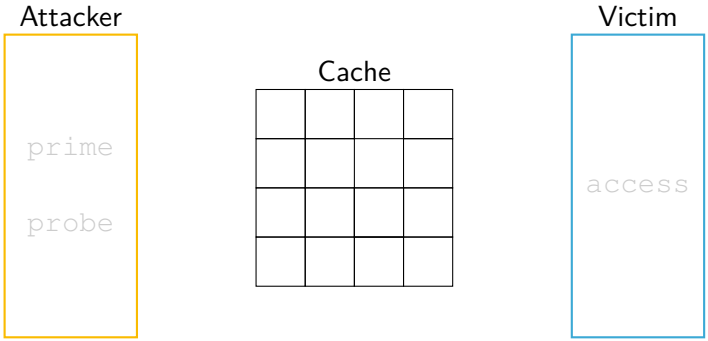

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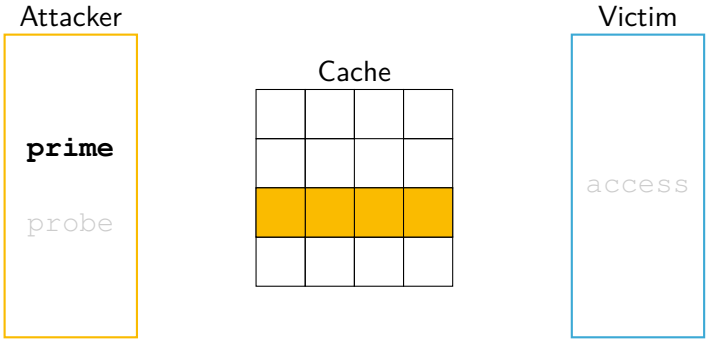

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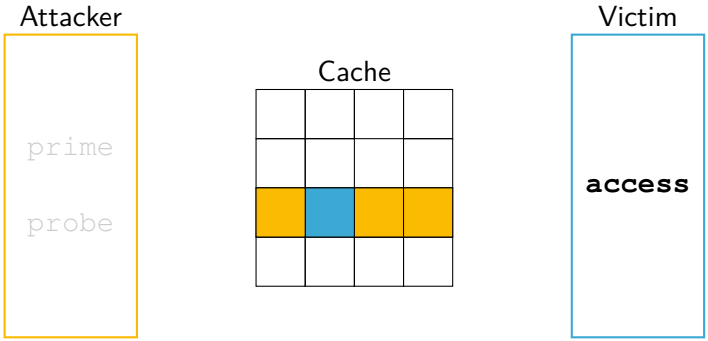

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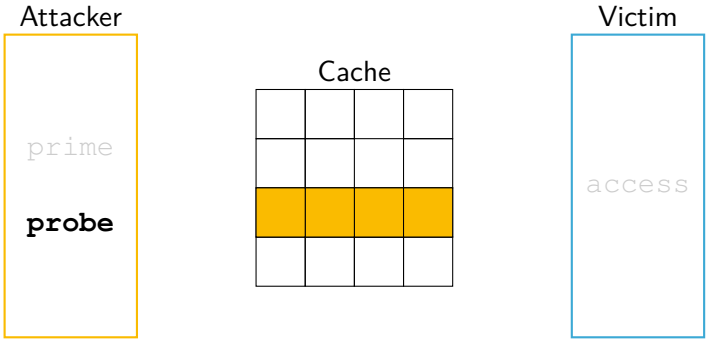

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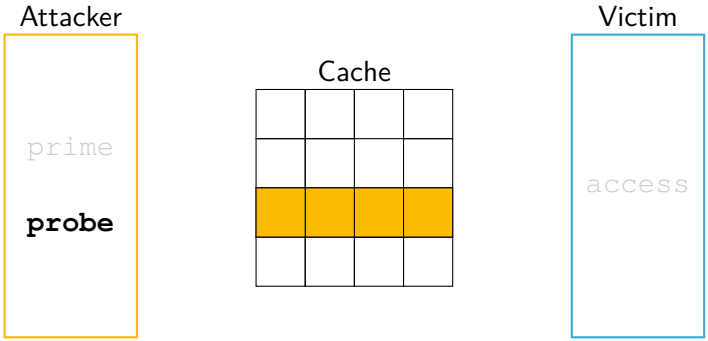
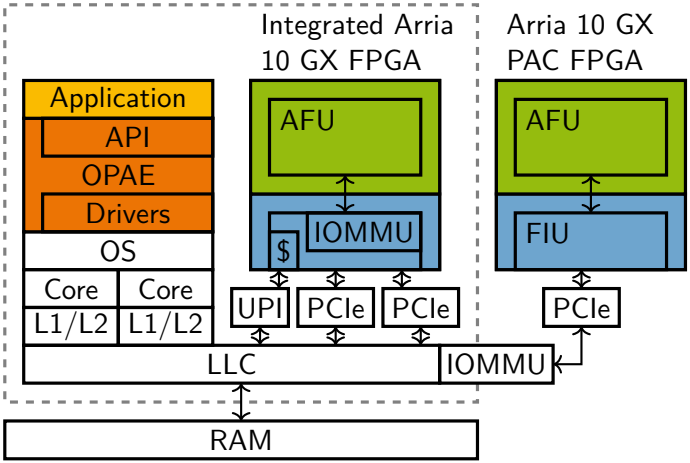


fast
Victim did not accessed

slow
Victim accessed

Cache Attacks

Attack Vectors – PCIe



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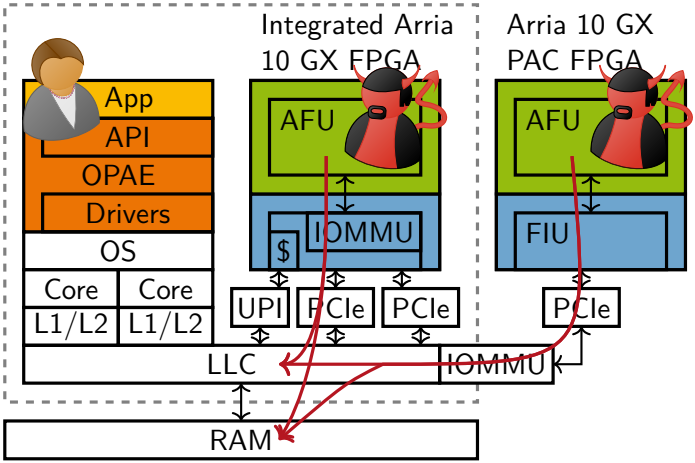

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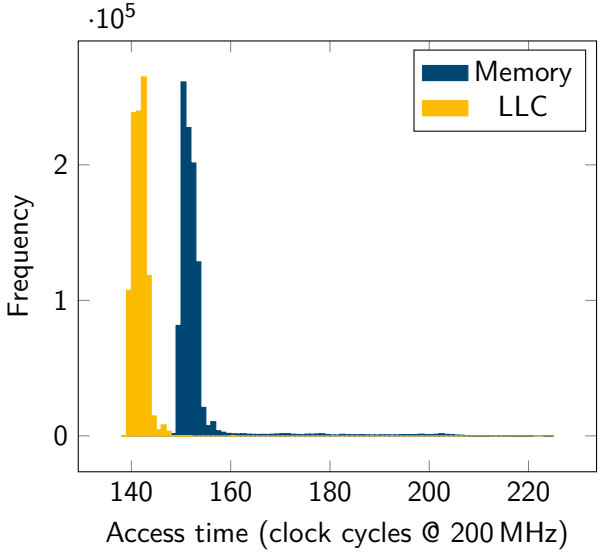

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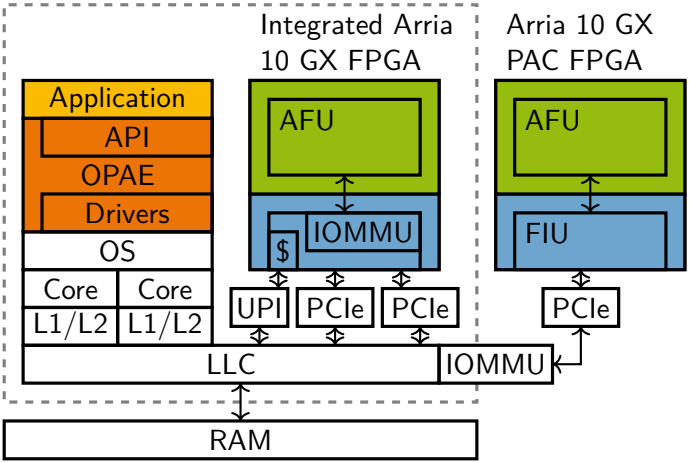
Attack Vectors – UPI



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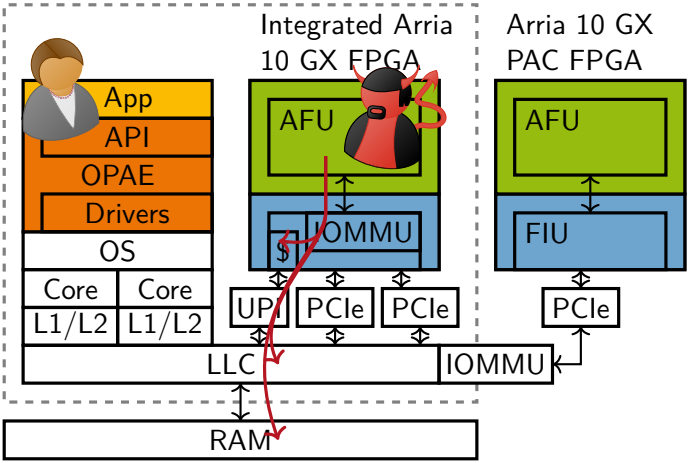
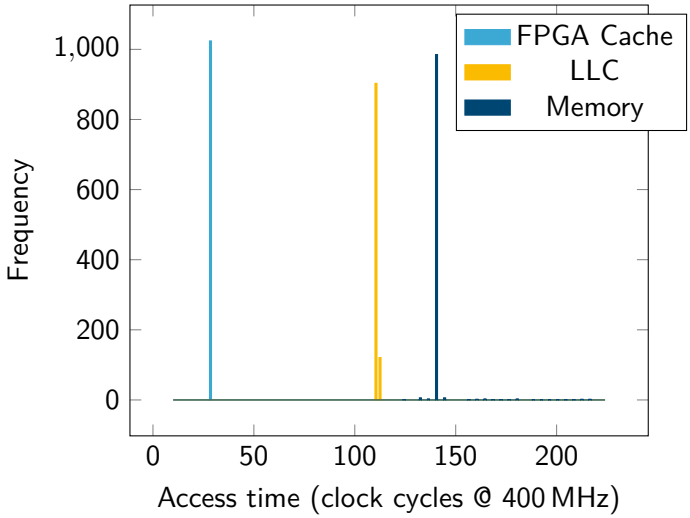


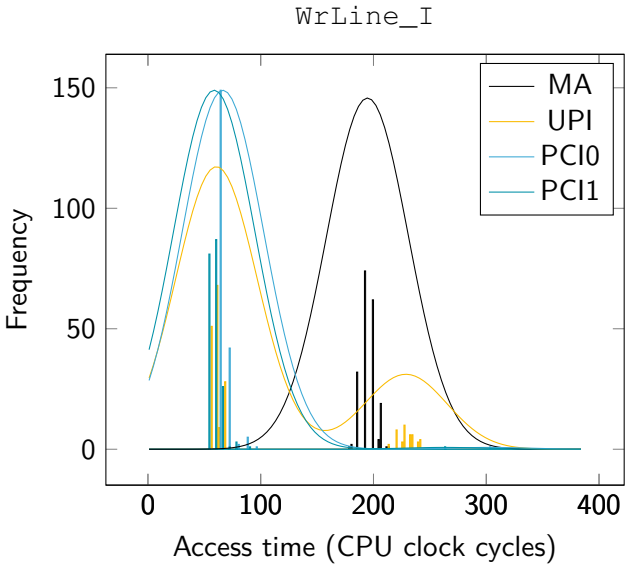
Cache Attacks

Attack Vectors – FPGA/UPI



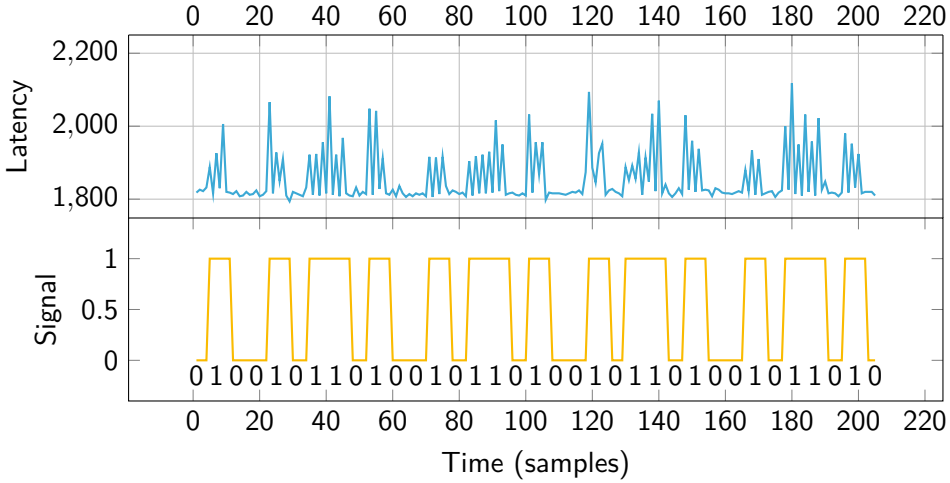
Cache Attacks

Attack Vectors – Caching Hints



Cache Attacks

Covert Channel



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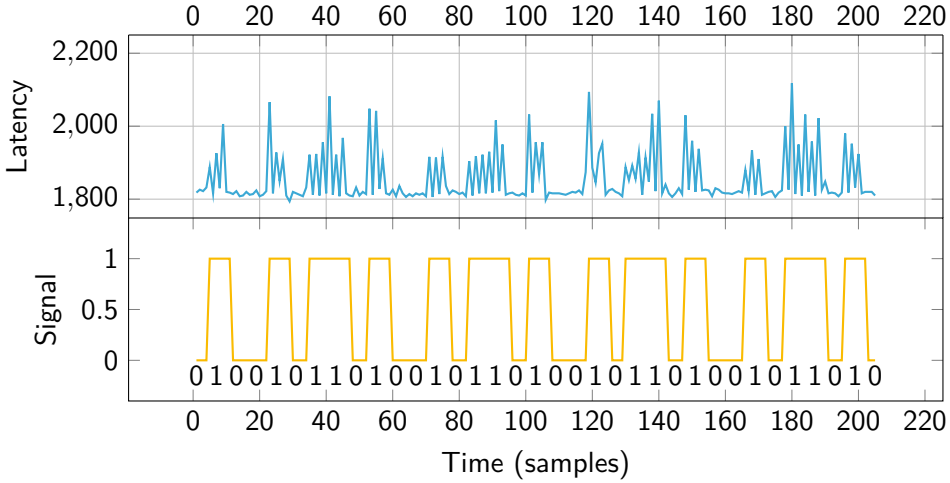

Throughput: 94.98 kBit/s

Cache Attacks

Summary of Cache Attack Analysis

Attacker	Target	Channel	Attack
FPGA PAC AFU	CPU LLC	PCIe	E+T, E+R, P+P
Integrated FPGA AFU	CPU LLC	UPI	E+T, E+R, P+P
Integrated FPGA AFU	CPU LLC	PCIe	E+T, E+R, P+P
CPU	FPGA Cache	UPI	F+R, F+F
Integrated FPGA AFU	FPGA Cache	CCI-P	E+T, E+R, P+P

JackHammer

Background – Rowhammer

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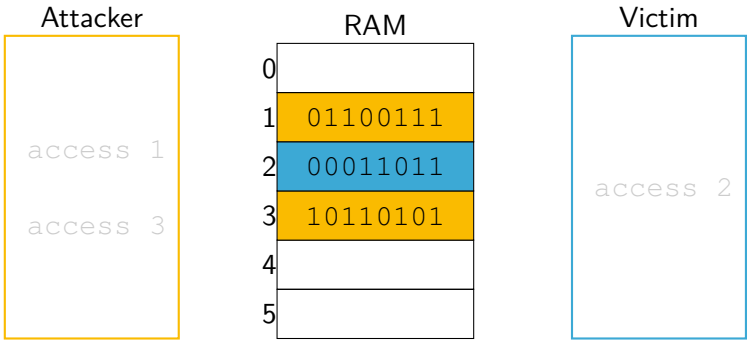

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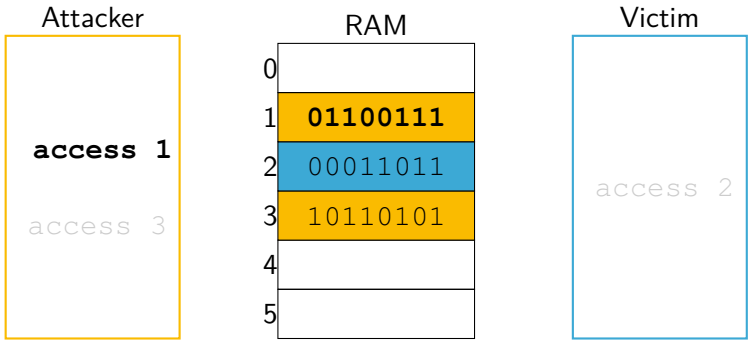

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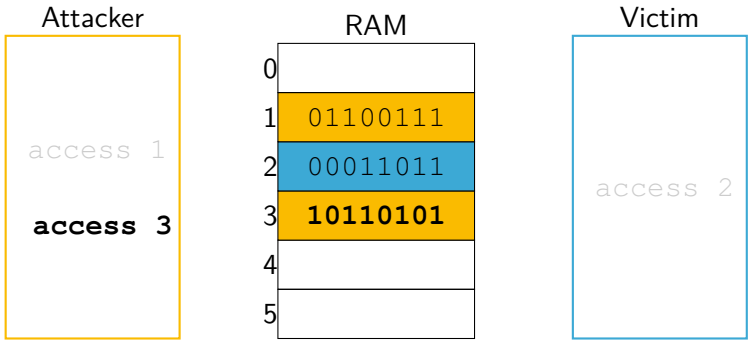

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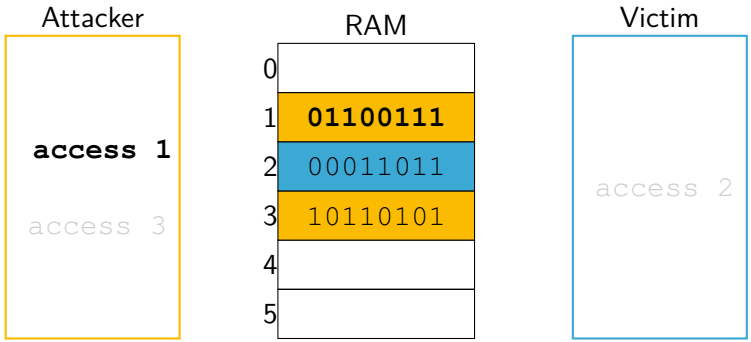

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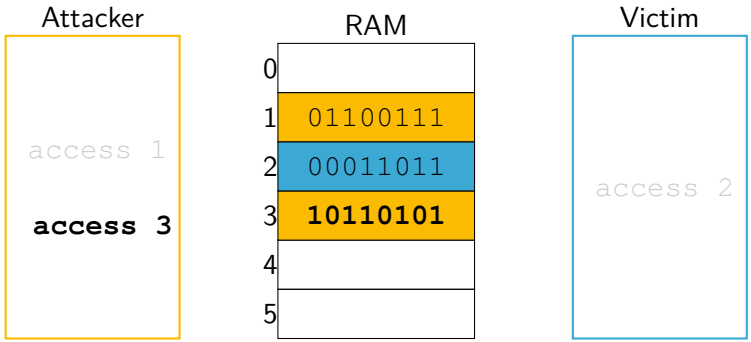

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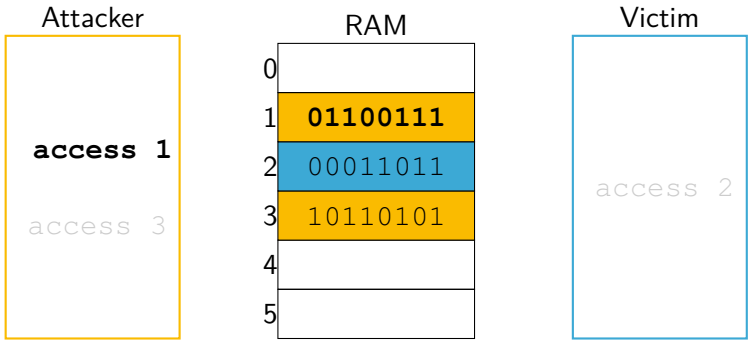

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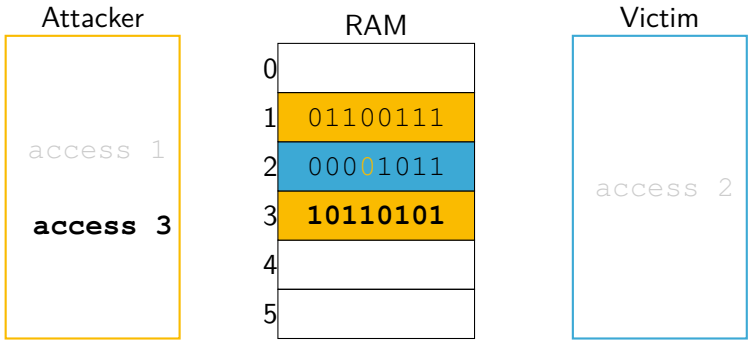

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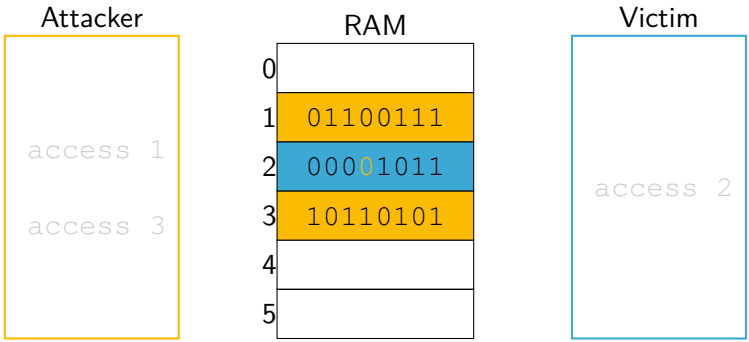

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JackHammer

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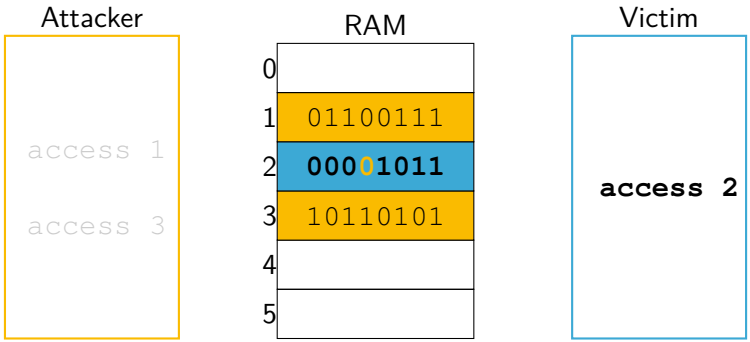

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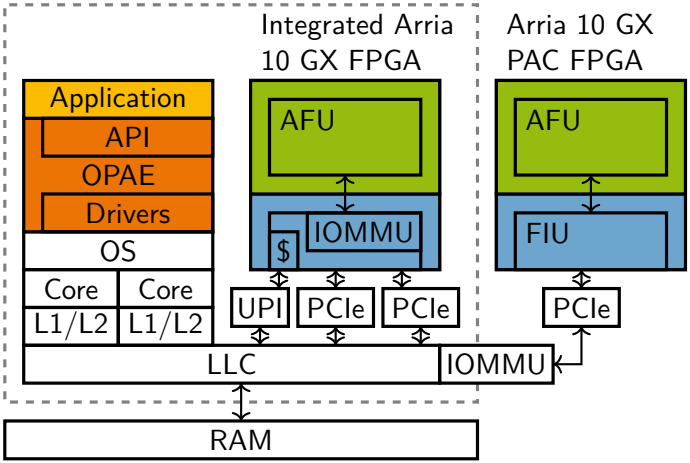
- Shown to work on many DDR3, some DDR4, some ECC

JackHammer

Background – Scenario



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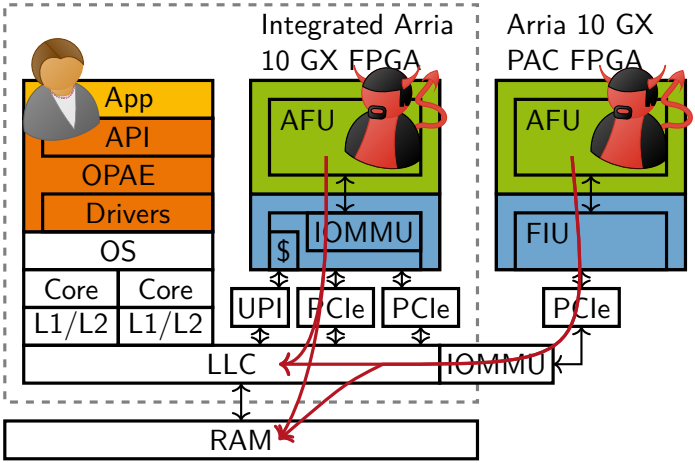

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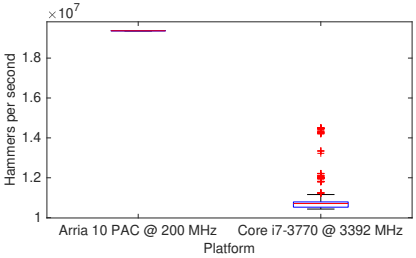
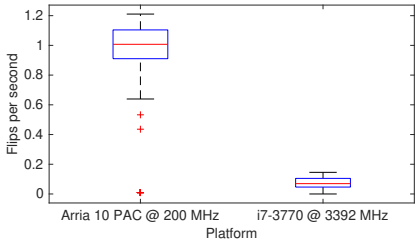
JackHammer

Performance

Hammering Rate



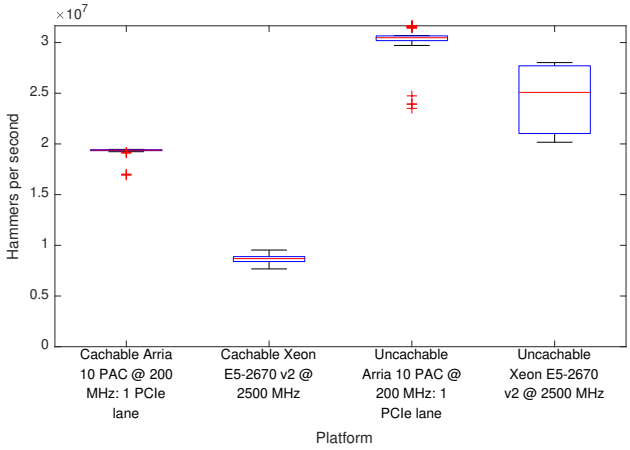
Flip Rate



JackHammer

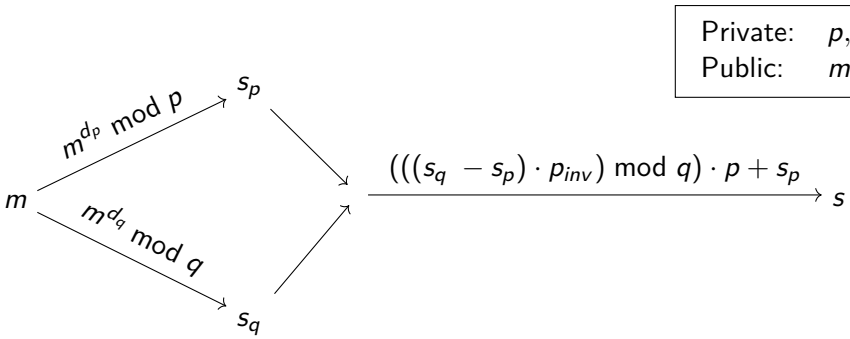
Caching and Rowhammer

Hammering rates with and without memory caching



JackHammer

RSA-CRT Fault Injection



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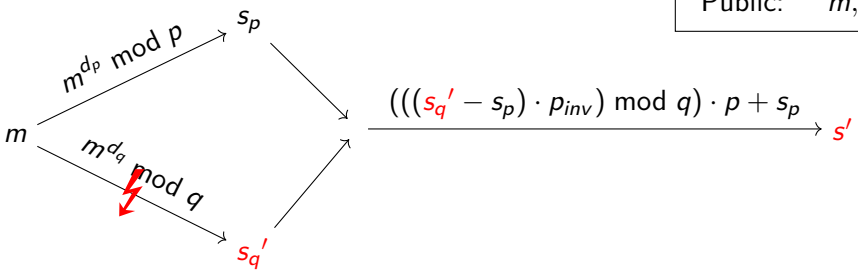

JackHammer

RSA-CRT Fault Injection

Private:	p, q, d_p, d_q
Public:	$m, s, N = pq$

$$
\begin{aligned}
& (((s'_q - s_p) \cdot p_{inv}) \bmod q) \cdot p + s_p \\
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\end{aligned}
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JackHammer

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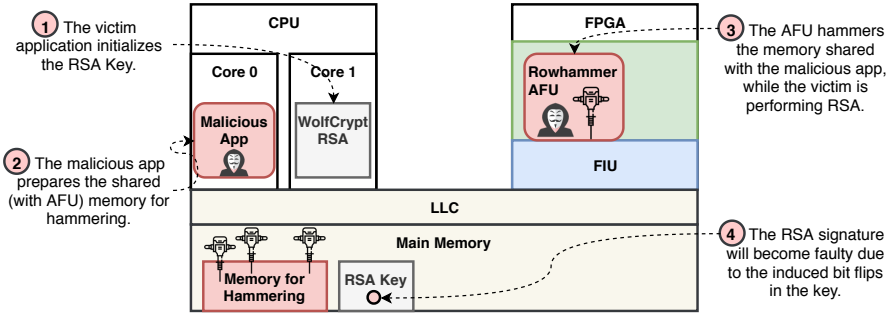
\end{aligned}
$$

Bellcore Attack:
$\Rightarrow \gcd(s' - s, N) = p$

JackHammer

End-to-End Fault Injection Attack (WolfSSL CVE-2019-19962)



JackHammer

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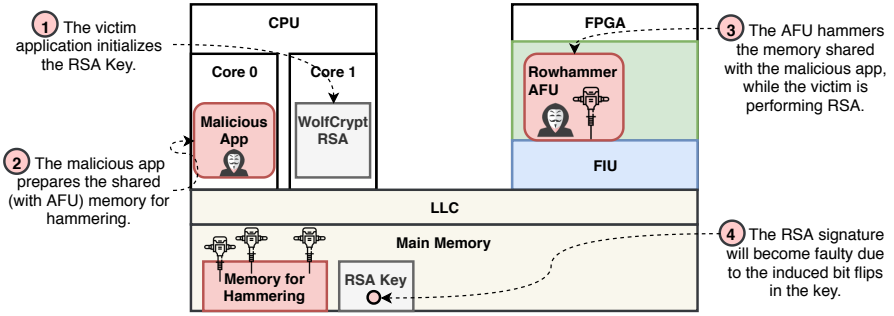

- Best case: JackHammer causes a fault 25% faster than CPU Rowhammer

JackHammer

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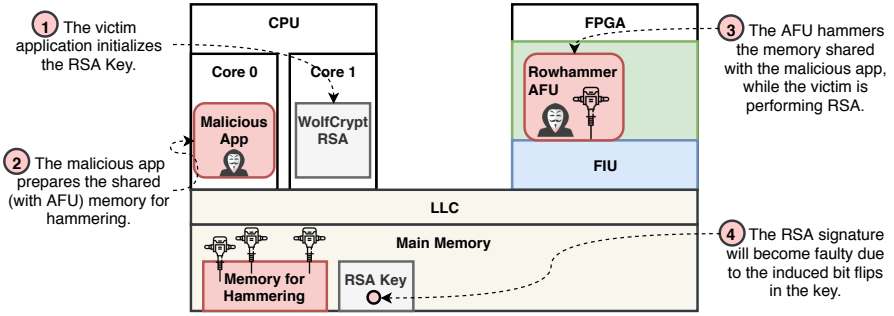

- Best case: JackHammer causes a fault 25% faster than CPU Rowhammer
- With doubled DRAM row refresh rate: 185% faster than CPU

Conclusions

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Acknowledgements

- Berk Sunar @ WPI
- Thomas Eisenbarth @ UzL
- Evan Custodio @ ex-Intel
- Alpa Trivedi @ Intel

Thanks for your attention!

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