riscure

The EXFILES project has received funding from the European Union's Horizon 2020 research and. innovation programme under grant agreement No 883156

Black box fuzzing with side channels

Sergei Volokitin

White box setting

- **Vulnerability research:**
  - **Source code review**
  - **Reverse engineering**
  - **Debugging**
  - **Fuzzing**
  - **etc.**

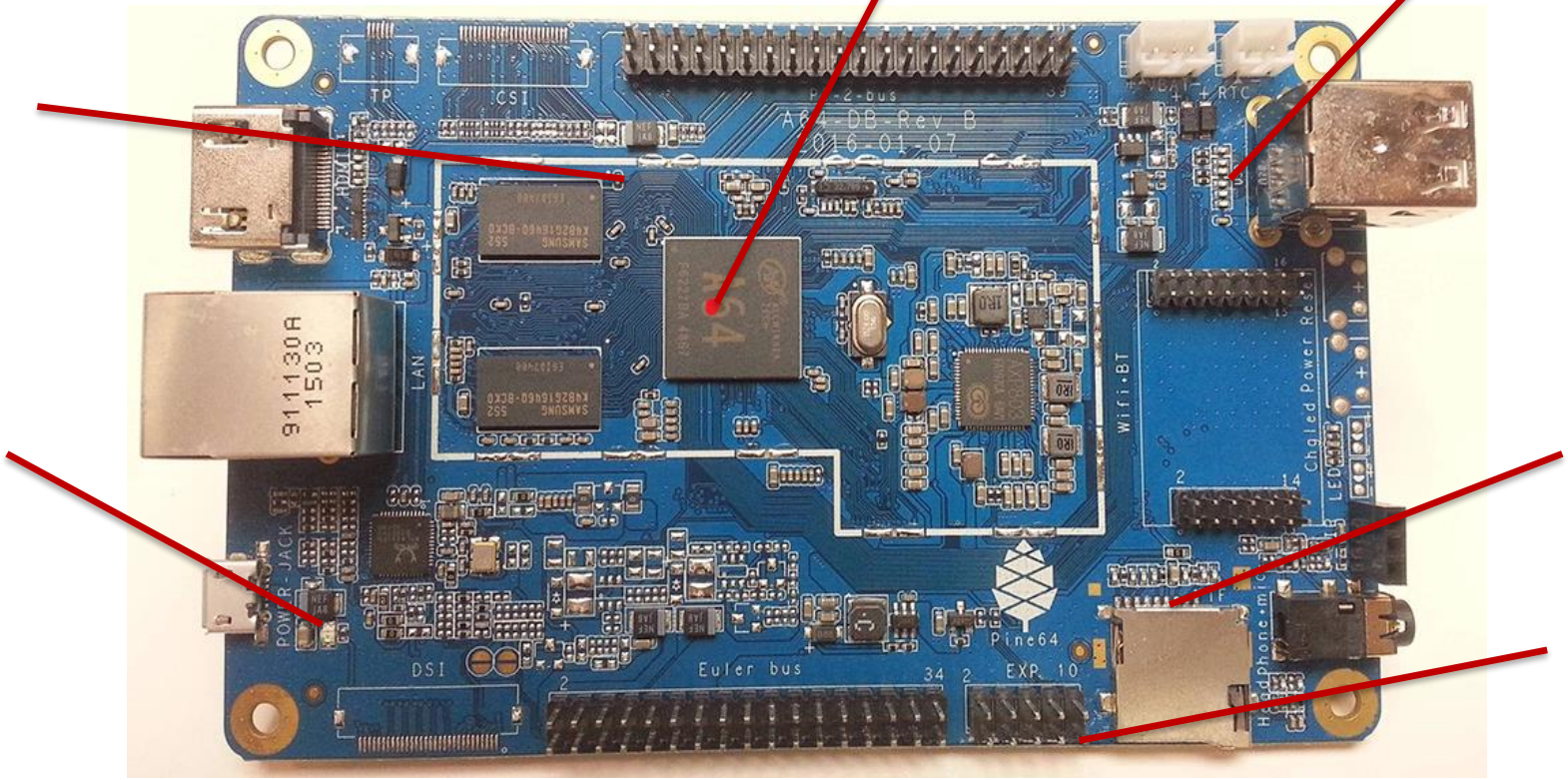
Black box setting

- Targets with limited/no public spec
- No source code
- No available binary
- Encrypted updates
- Protected memory
- No debug

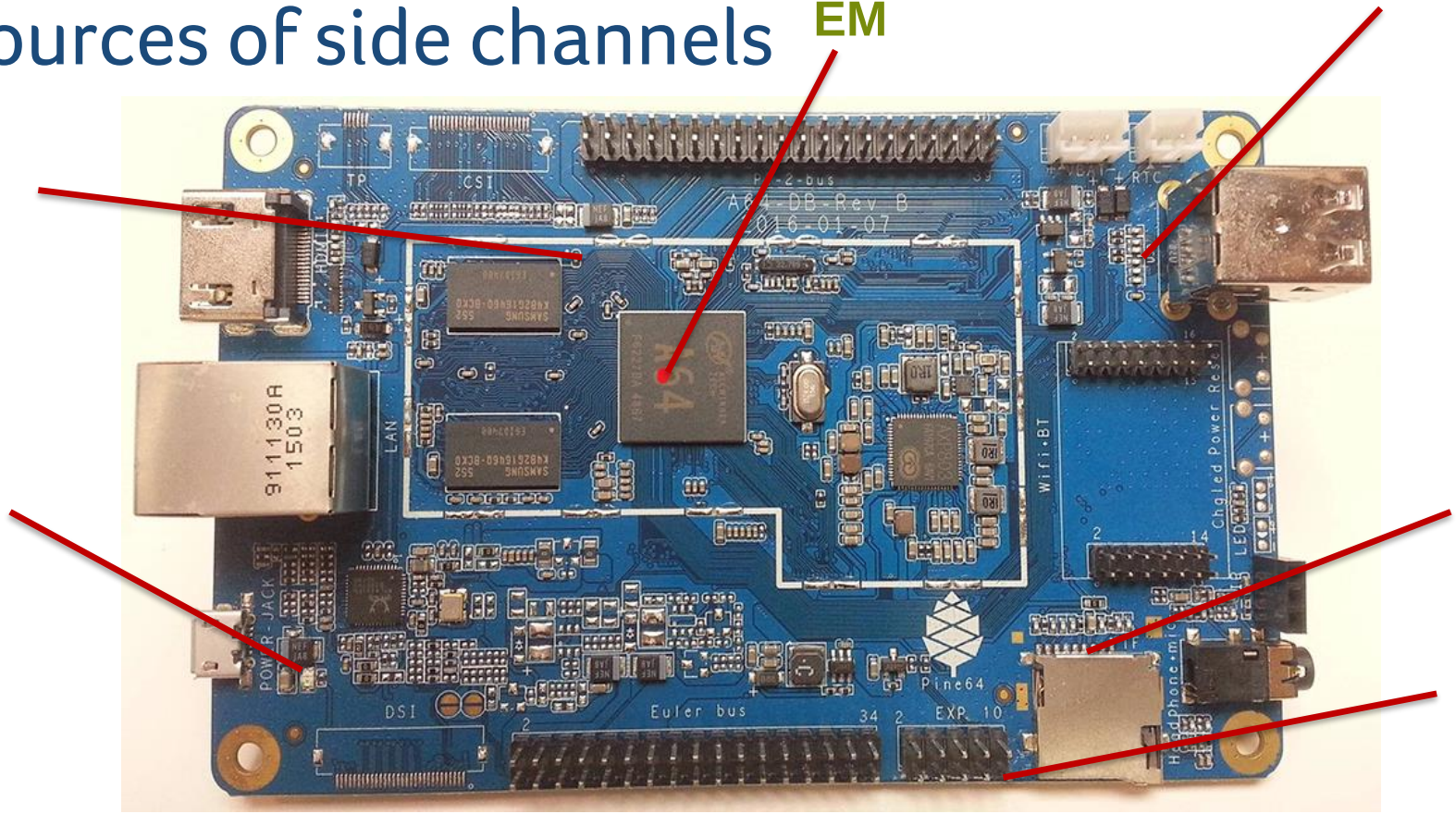
Fuzzing with side channels

Can we explore black box targets more efficiently by leveraging physical access to the target?

Sources of side channels



Sources of side channels



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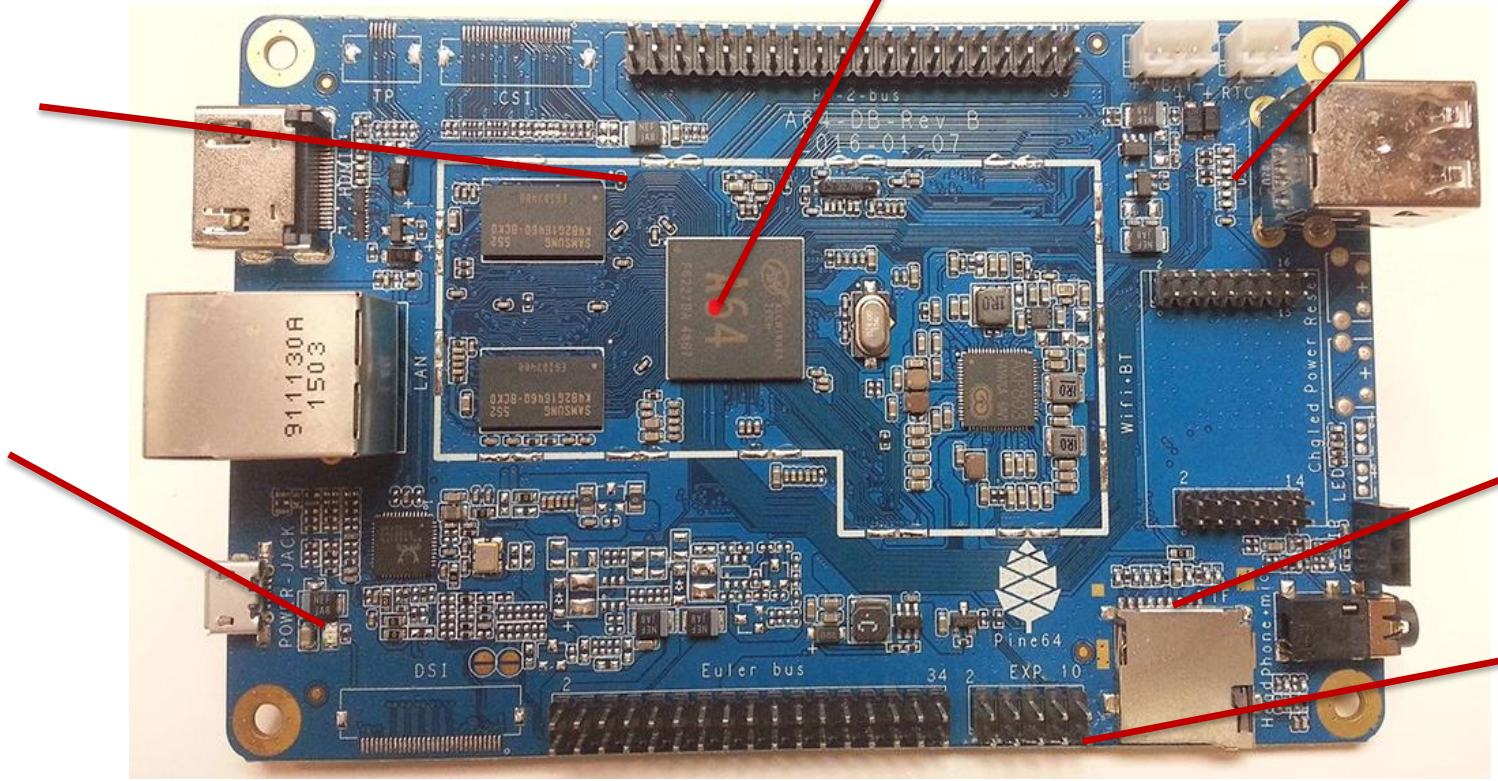
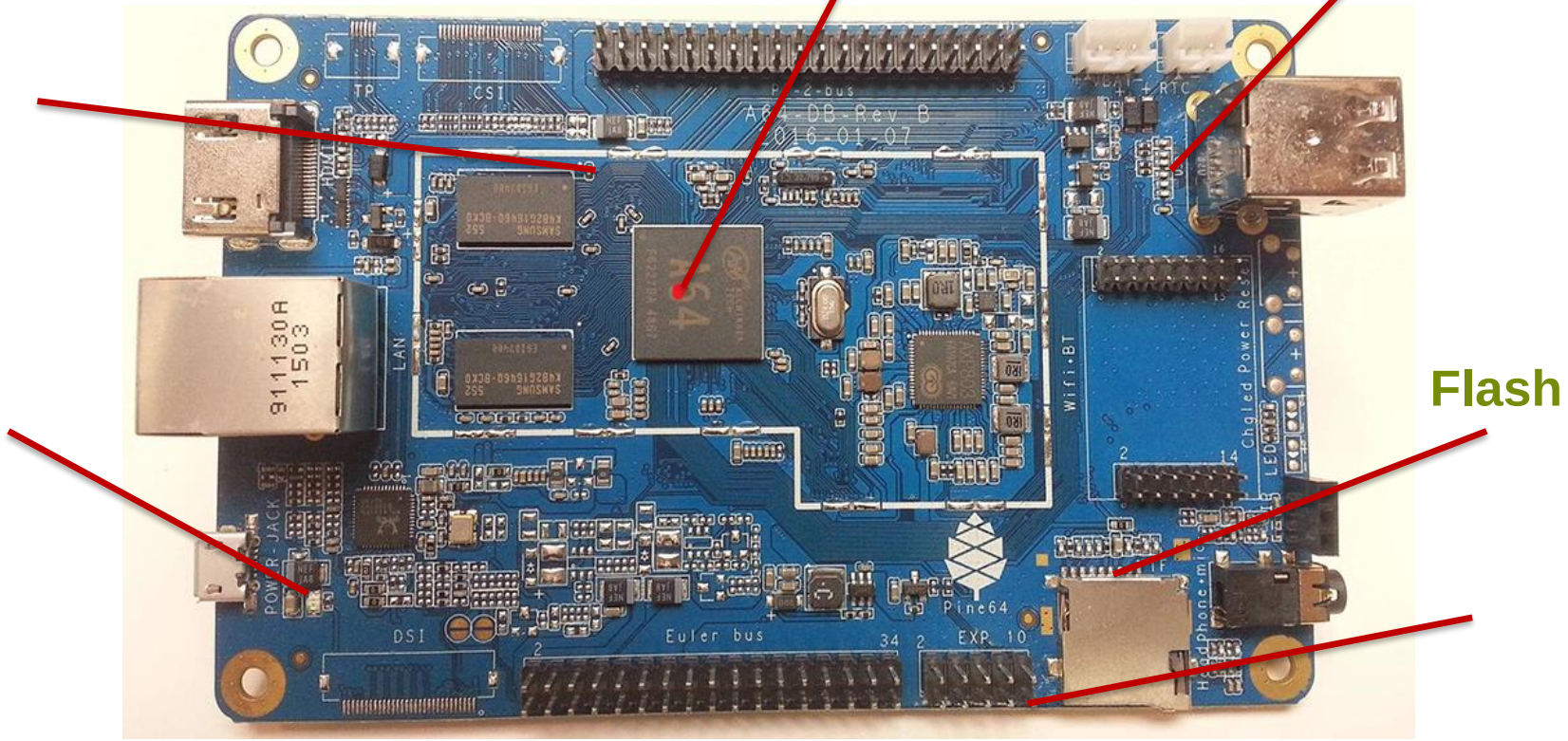
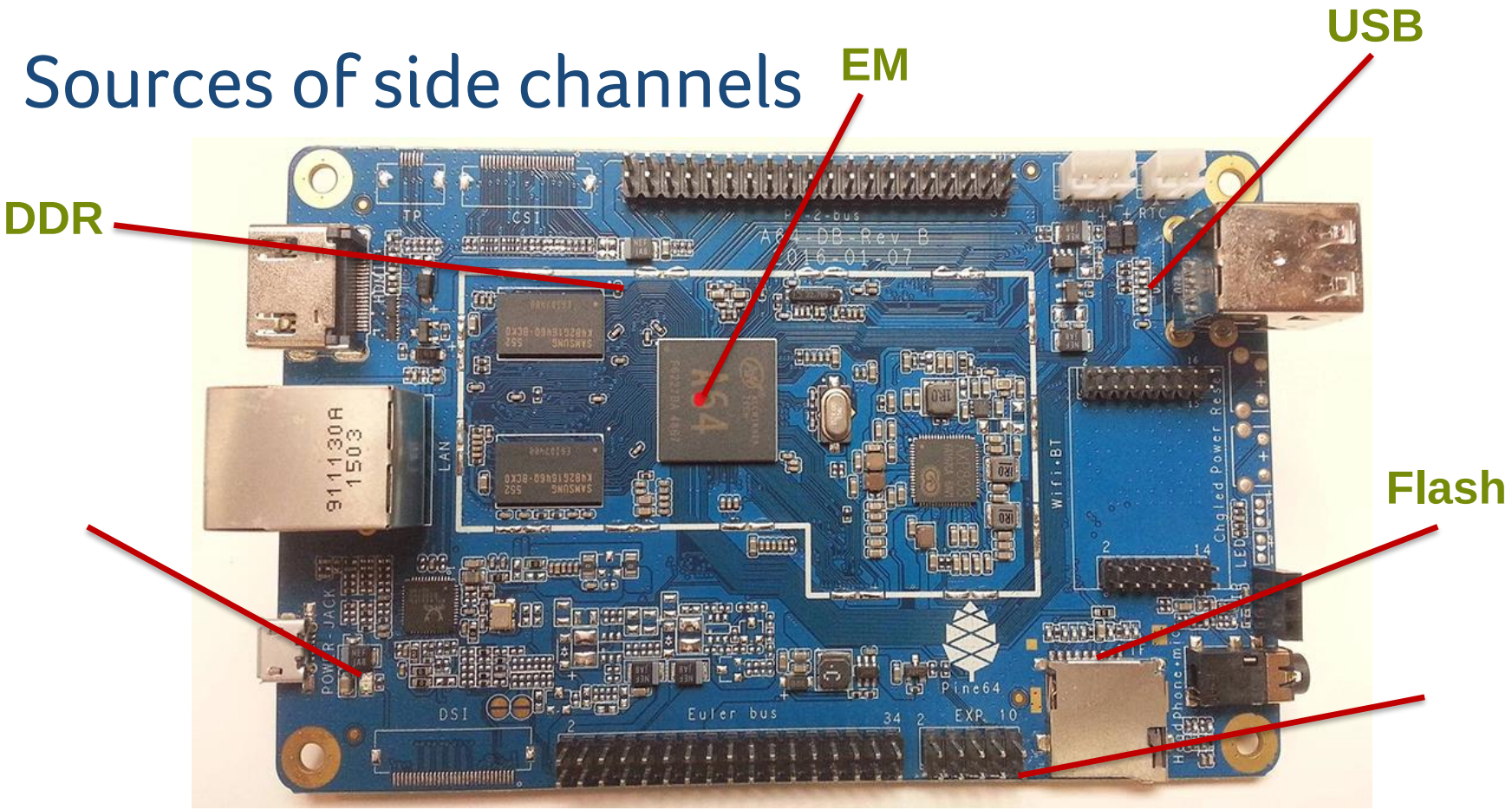


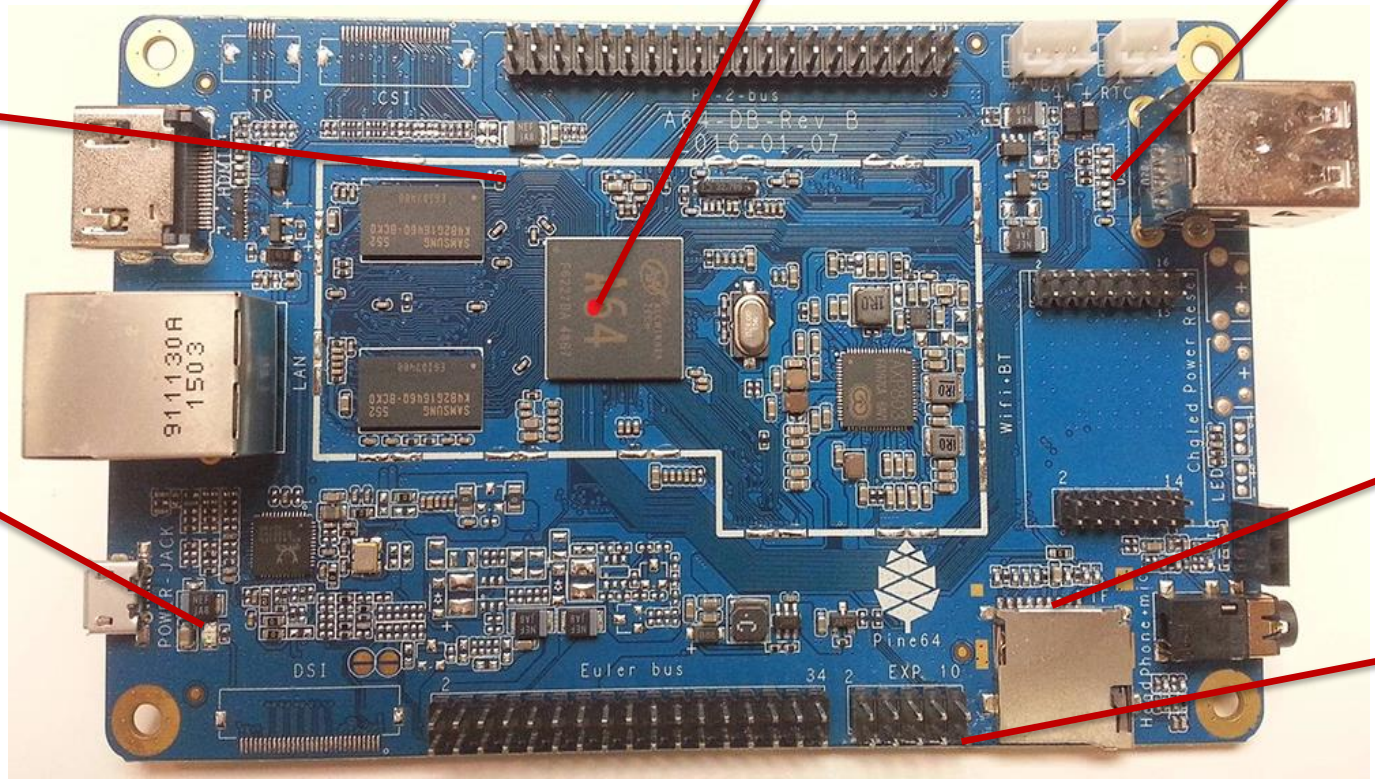
Sources of side channels



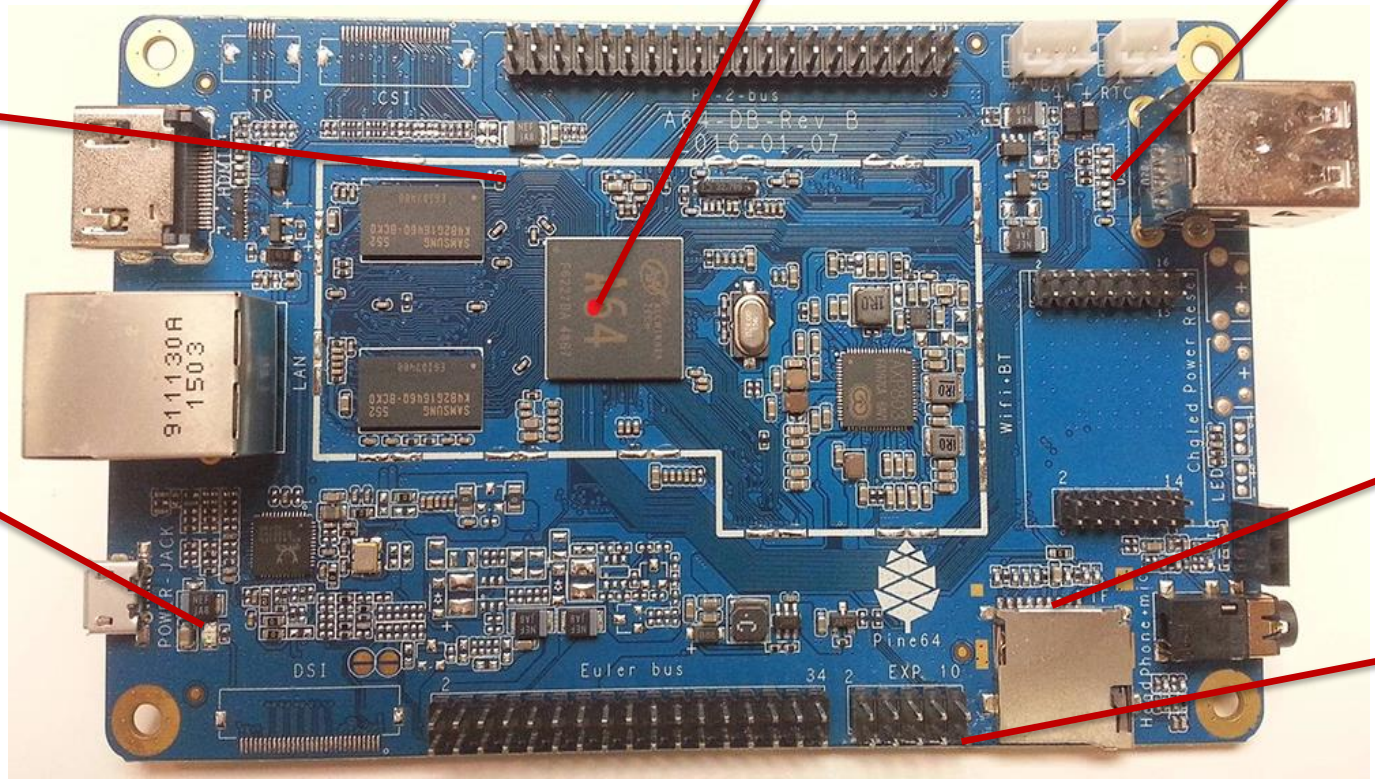
Sources of side channels



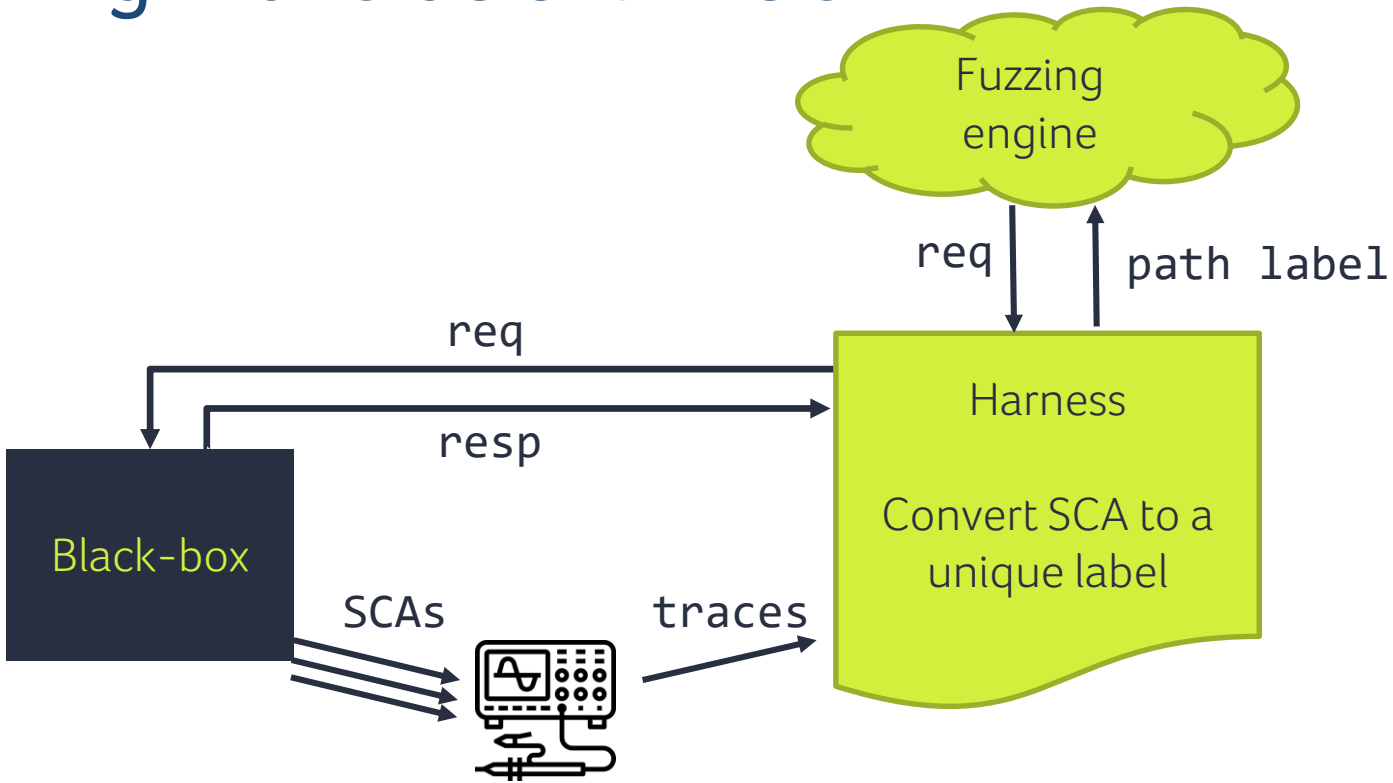
Sources of side channels



Sources of side channels



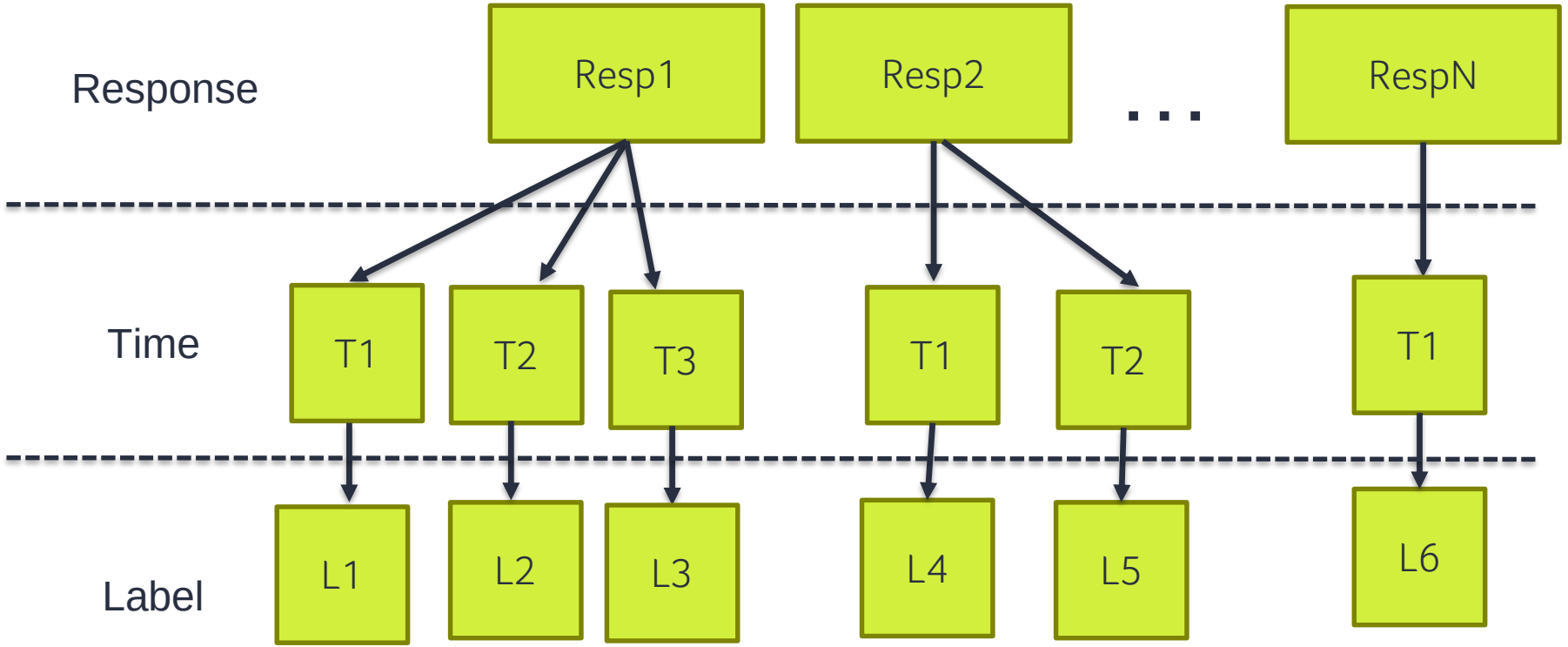
Fuzzing with side channels



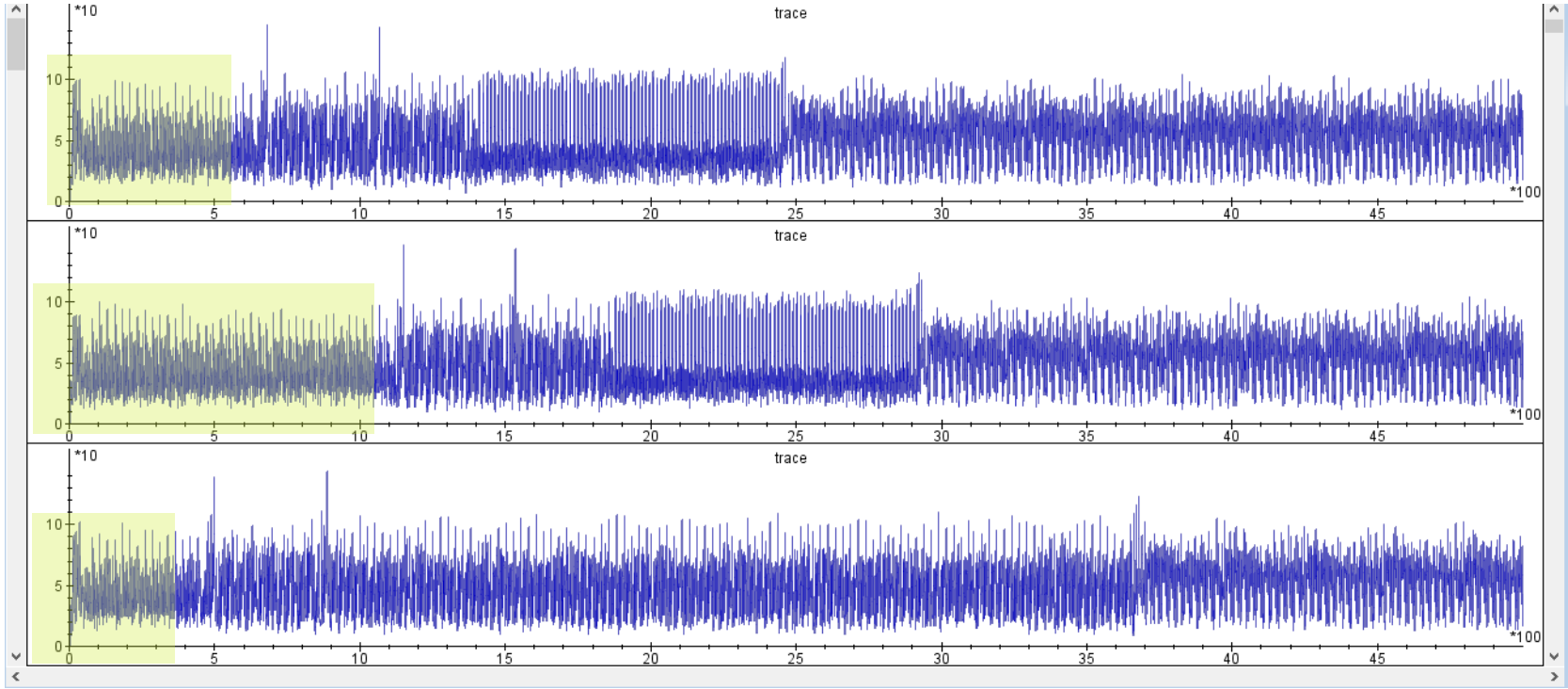
Fuzzing with side channels approach

- Types of side channels:
  - Response data, timing, power trace, EM trace, serial memory access, GPIO activity…
- Hierarchy of sources
  - Not all the SCA data has equal priority of labeling
  - Response → Serial → Timing → Power/EM trace
- Extendable Hierarchical Labeler

Extendable Hierarchical Labeler



Jitter and labelling



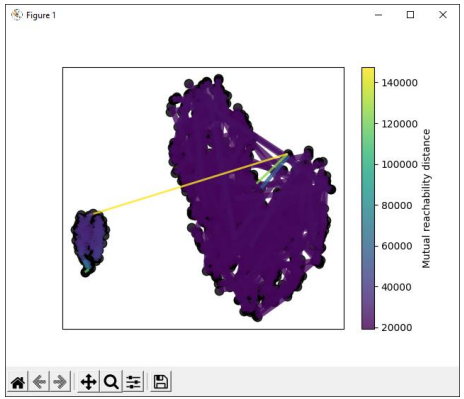
Trace labelling challenges

- Trace labelling
  - We perform clustering
  - The data is noisy
  - Need to cluster traces incrementally
  - Need to do it sufficiently fast

Jitter effects on clustering - HDBSCAN

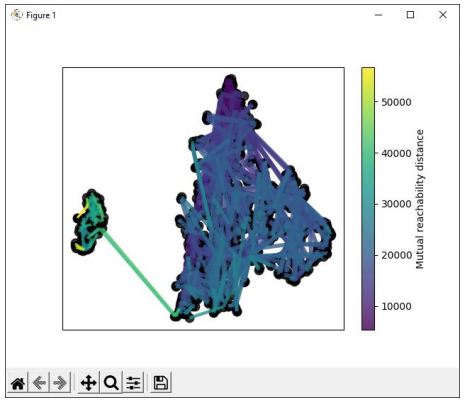
- **Synthetic tests of two commands with a different amount of jitter in the signal**

0%



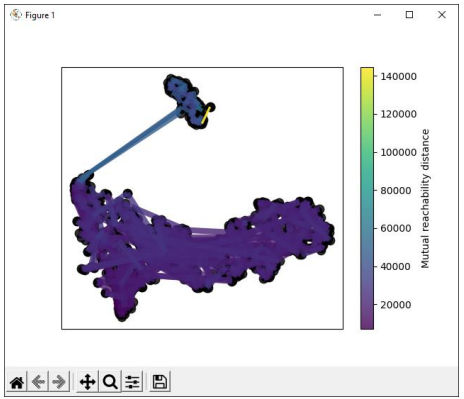
Mislabeled 0.1%

10%



Mislabeled 1.7%

20%

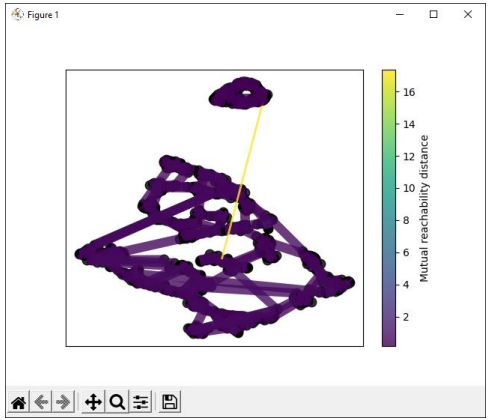


Mislabeled 3.8%

Jitter effects on clustering - UMAP

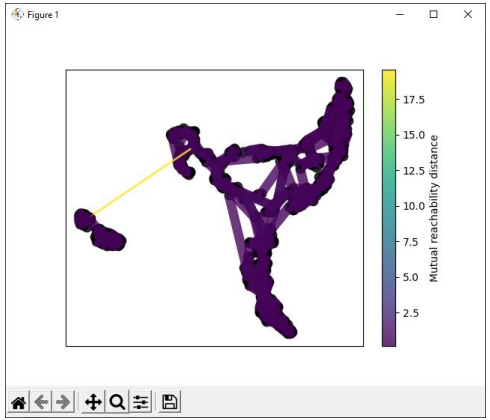
- **UMAP + HDBSCAN**

0%



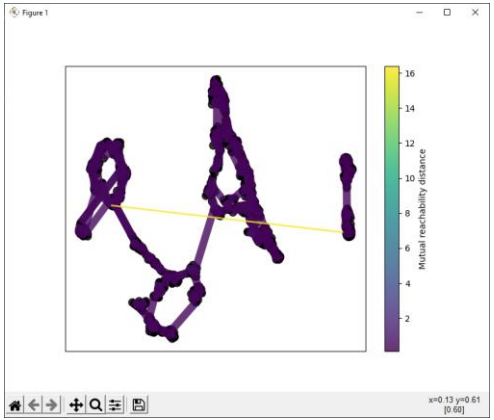
Mislabeled 0.1%

10%



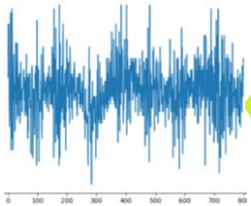
Mislabeled 0.8%

20%

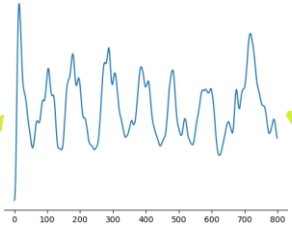


Mislabeled 0.9%

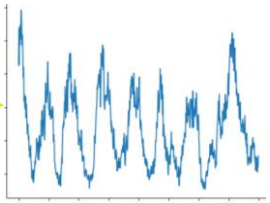
Power trace labelling



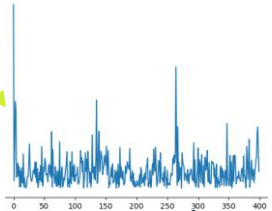
EM / Power



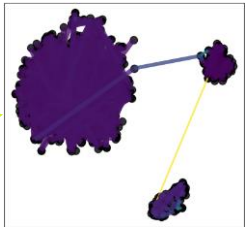
Low pass



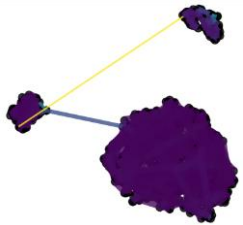
Moving average



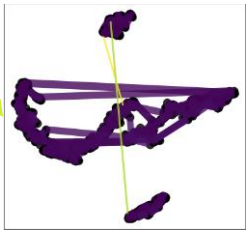
Frequencies



HDBSCAN



PCA+HDBSCAN



UMAP+HDBSCAN

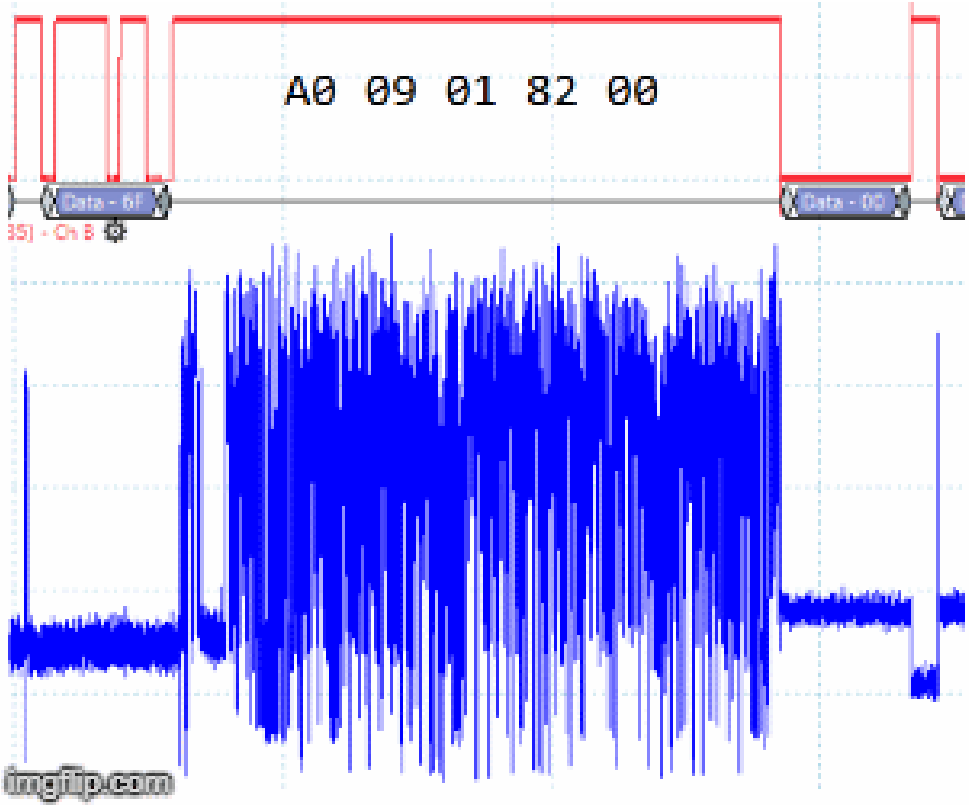
Smart Card Use case

- **Apply the fuzzing method to a smart card applet**
- **Self written code, can assess the coverage**
- **Only 0x9000 SW is returned, no data**

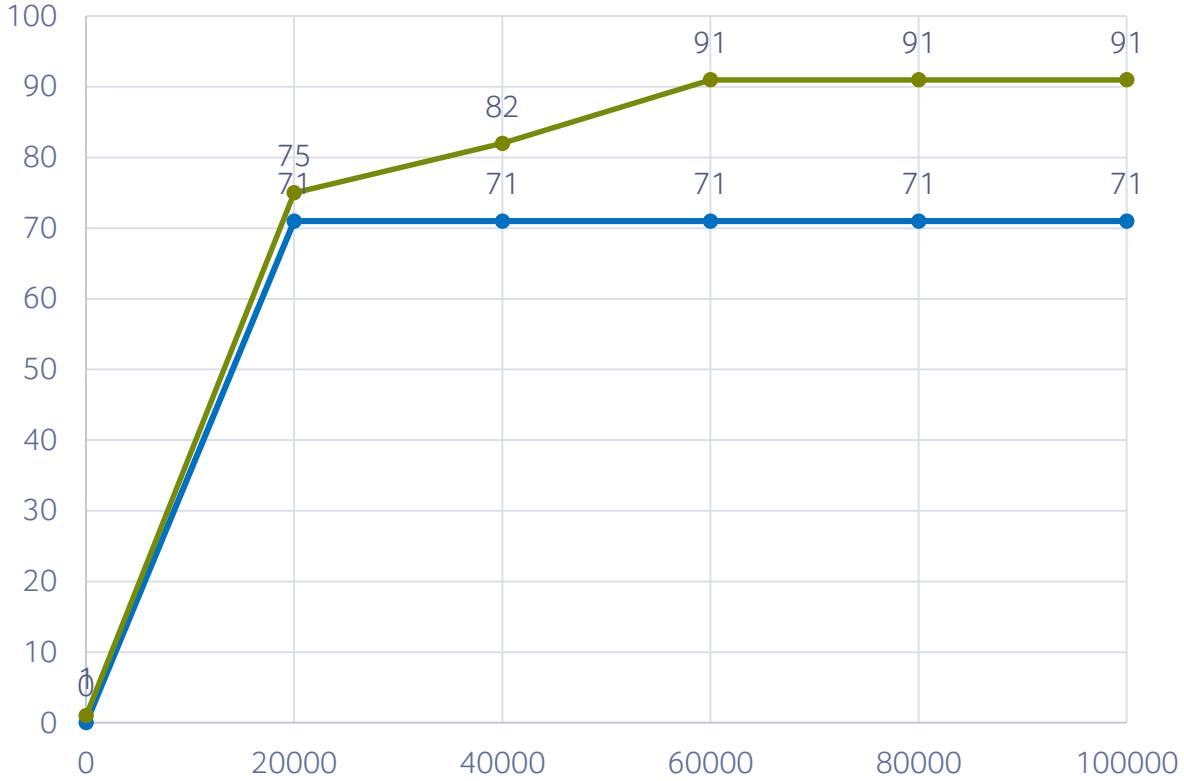
Applet code

```
74    switch(buffer[ISO7816.OFFSET_INS]) {
75
76      case INS_PATH_1: // THROW 0x9000
77        ISOException.throwIt(ISO7816.SW_NO_ERROR);
78        break;
79
80      case INS_PATH_2: // FILL TRANSIENT ARRAY WITH ZEROS
81        Util.arrayFillNonAtomic(transArr, (short)0, (short)transArr.length, (byte) 0x00);
82        ISOException.throwIt(ISO7816.SW_NO_ERROR);
83        break;
84      ...
85      case INS_PATH_4: // FILL TRANSIENT ARRAY WITH ZEROS DEPENDING ON THE INPUT
86        c = Util.getShort(buffer,(short)ISO7816.OFFSET_CDATA);
87        Util.arrayFillNonAtomic(transArr, (short)0, c, (byte) 0x00);
88        ISOException.throwIt(ISO7816.SW_NO_ERROR);
89        break;
90      ...
91      case INS_PATH_6: // FILL PERSISTENT ARRAY WITH ZEROS DEPENDING ON THE INPUT
92        c = Util.getShort(buffer, (short)ISO7816.OFFSET_CDATA);
93        for (c = 0; c < 32; c++) {
94          if (buffer[(short)(ISO7816.OFFSET_CDATA + c)] != secret[c]) {
95            break;
96          }
97        }
98        ISOException.throwIt(ISO7816.SW_NO_ERROR);
99        break;
```

Power traces

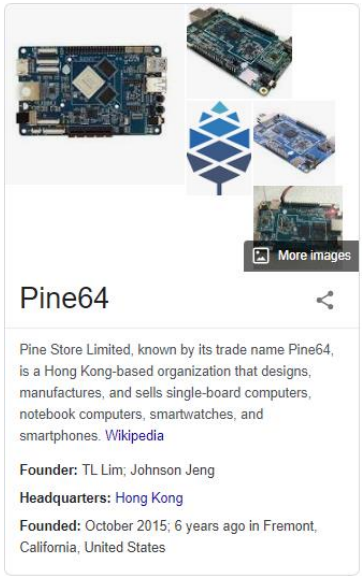


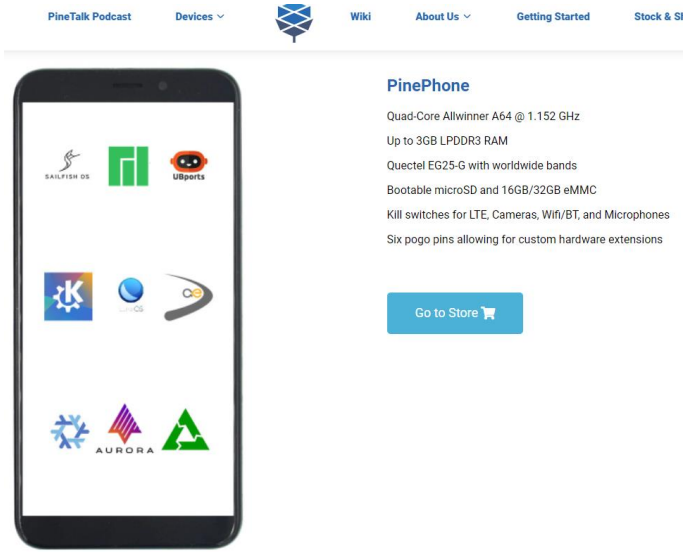
Coverage: Random vs Fuzzer



Smart phone use case

- **Apply the fuzzing method to Uboot of PinePhone**



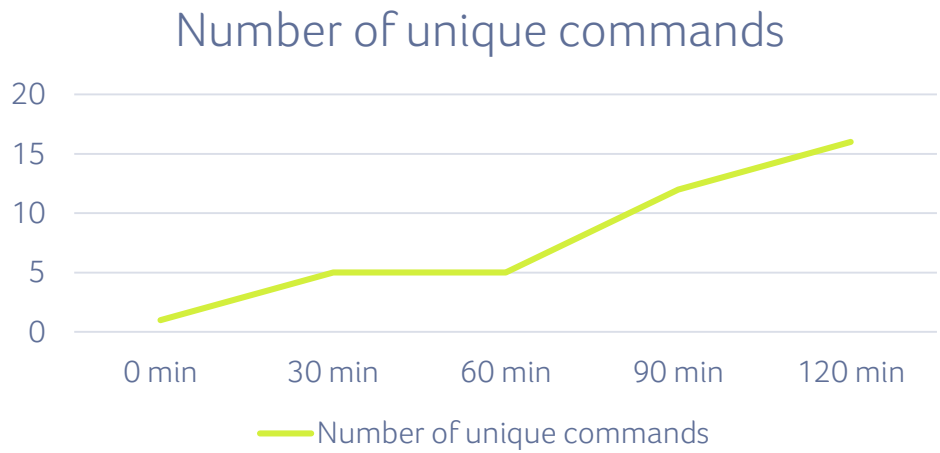


Smart phone use case

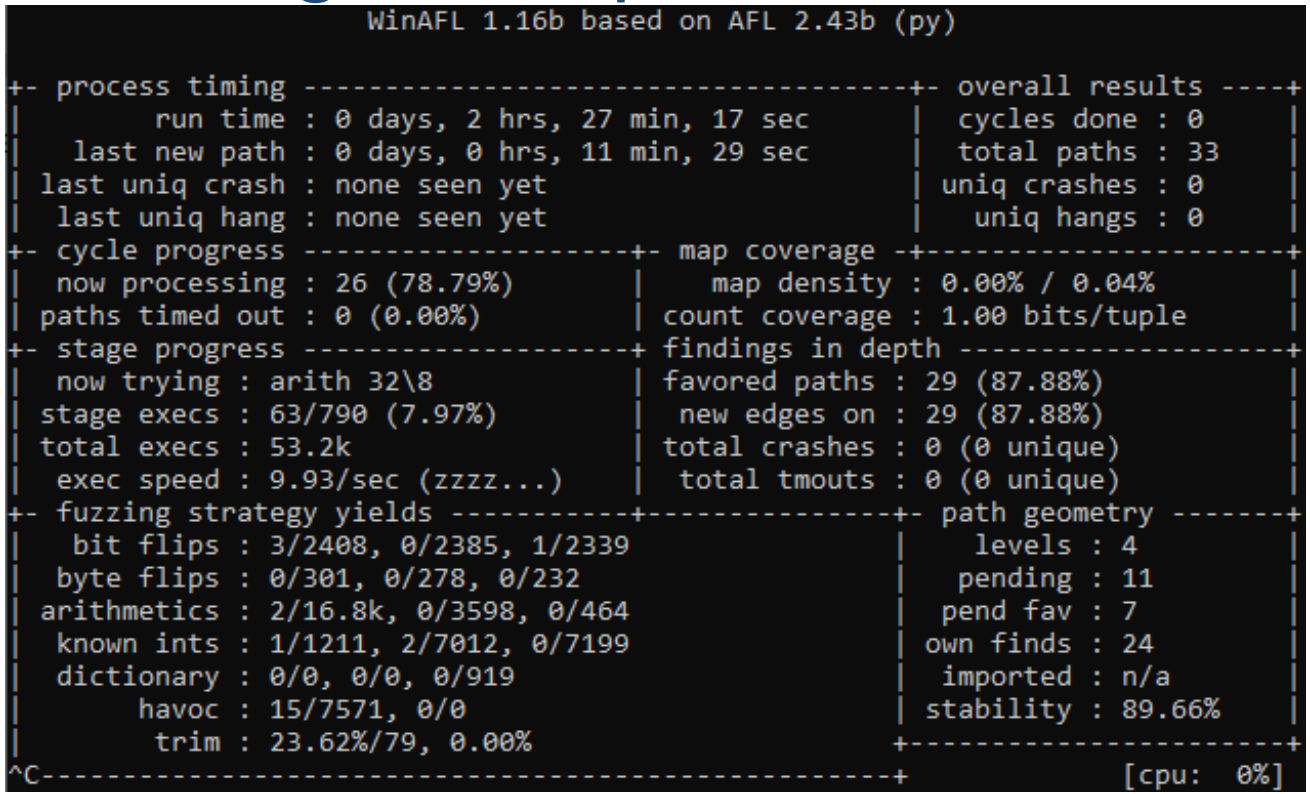
- **Apply the fuzzing method to Uboot of PinePhone**
- **Available docs and source code for verification**
- **Real life, but not the most secure implementation**

No Corpus case

- Started with empty corpus
- responses and timing
- No help to the fuzzer
- Responses are verbose
- 16 CMDs in 2h
- ~6 execs per second



Uboot fuzzing, no corpus case

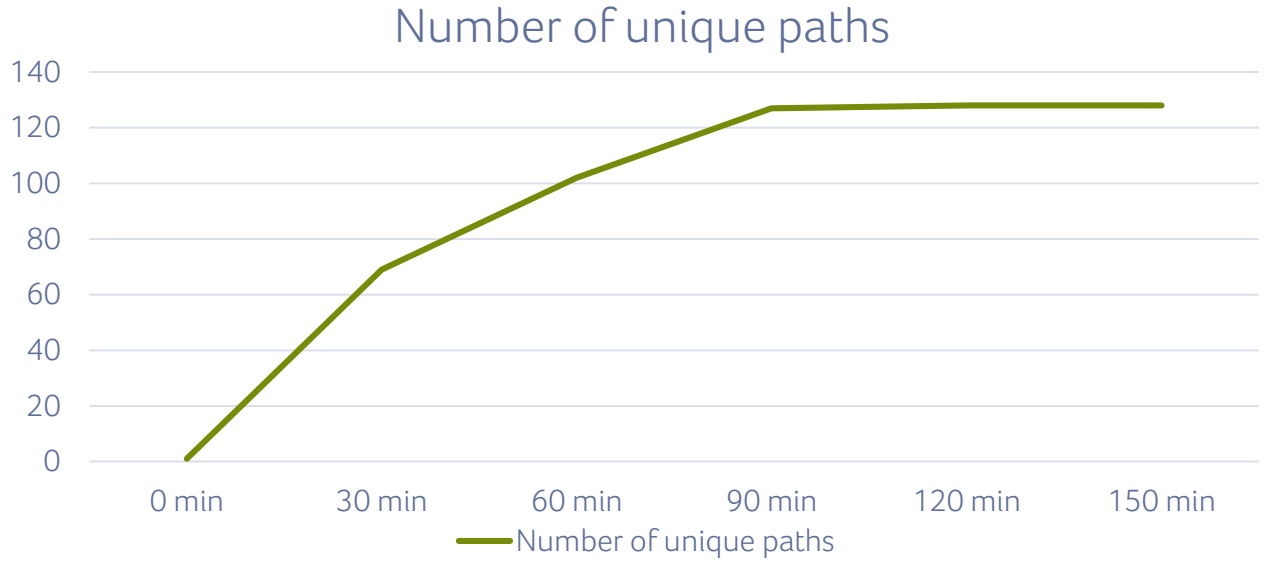


U-Boot with all the commands in the corpus

- Started with all of the available commands
- Corpus has correct syntax
- Fuzzer finds commands independently
- Crashes

U-Boot with all the commands in the corpus

- **State explosion**
- **Syntax errors**



U-Boot crashes

```
UART cmd:

    b'md Fd \x7f'

Response:
000000fd:"Synchronous Abort" handler, esr 0x96000021
ELR:     bff91c84
LR:      bff91c60
x0 : 00000000bbf3d058 x1 : 0000000000000000
x2 : 000000000000003a x3 : 00000000000000fd
x4 : 00000000bbf3cb10 x5 : 0000000000000004
x6 : 0000000000000001 x7 : 000000000000000f
x8 : 00000000bbf3ceb0 x9 : 0000000000000008
x10: 00000000bbf3cb19 x11: 0000000000000021
x12: 0000000000000008 x13: 00000000ffffffff
x14: 00000000bbf3d2ac x15: 00000000bbf3d378
x16: 00000000bff62954 x17: 0000000000000000
x18: 00000000bbf40df8 x19: 0000000000000040
x20: 00000000000000fd x21: 00000000000000fd
x22: 0000000000000004 x23: 00000000bffa7688
x24: 0000000000000008 x25: 0000000000000009
x26: 0000000000000004 x27: 0000000000000004
x28: 0000000000000000 x29: 00000000bbf3cfd0

Resetting CPU ...

resetting ...

```

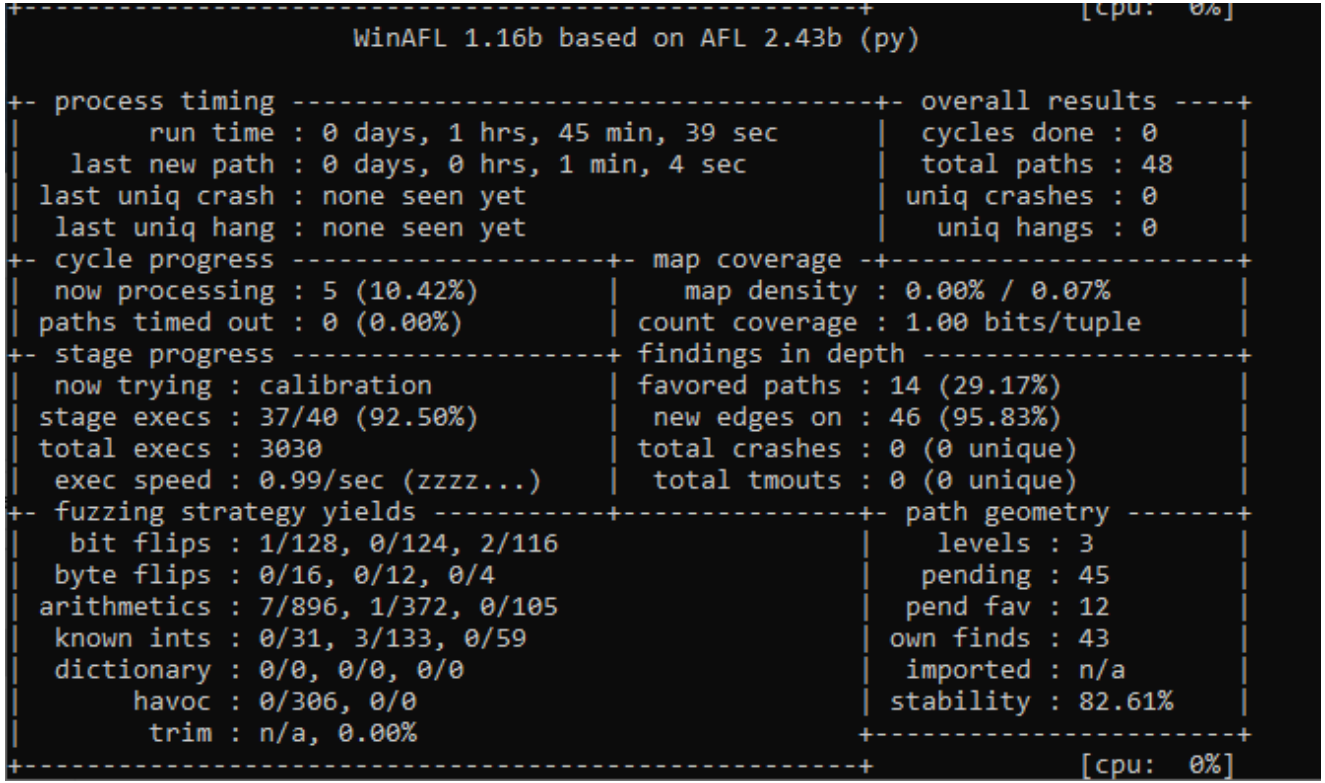
CRC32 command use case

- `crc32 0x40000000 0x4000`
- `CRC 40000000 … 40003fff => 0xbf13d15a`

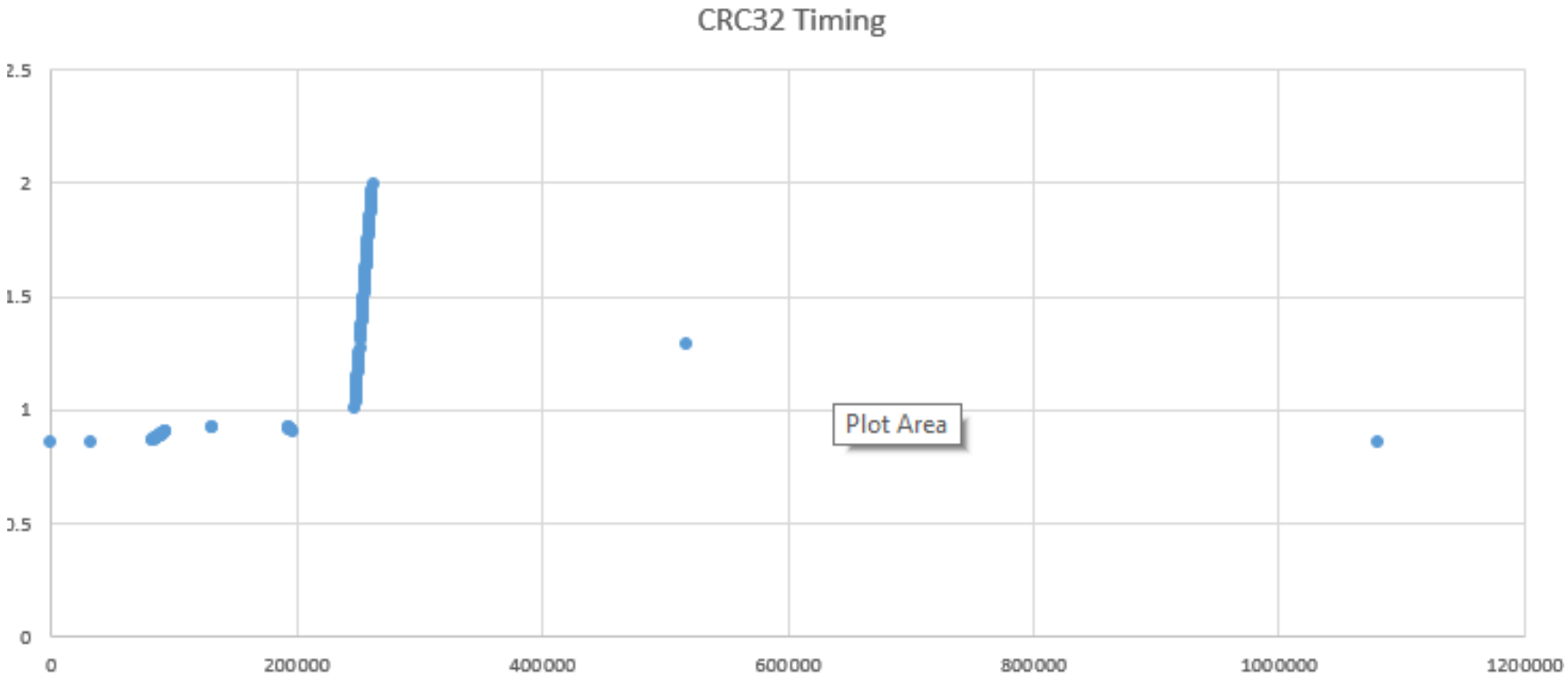
- Initial run produced 16 different labels
- The returned data was different

- … but the timing also differs

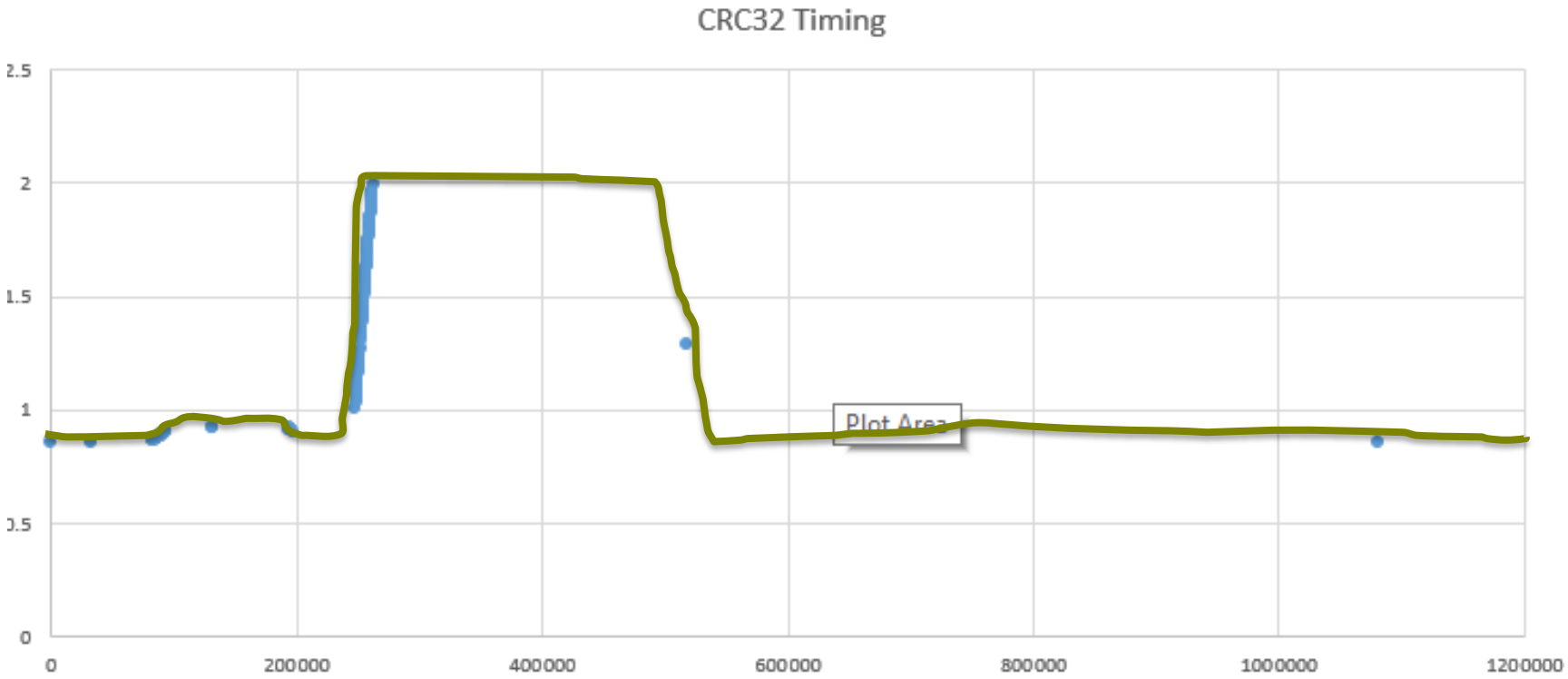
CRC32 command use case



CRC32 command use case



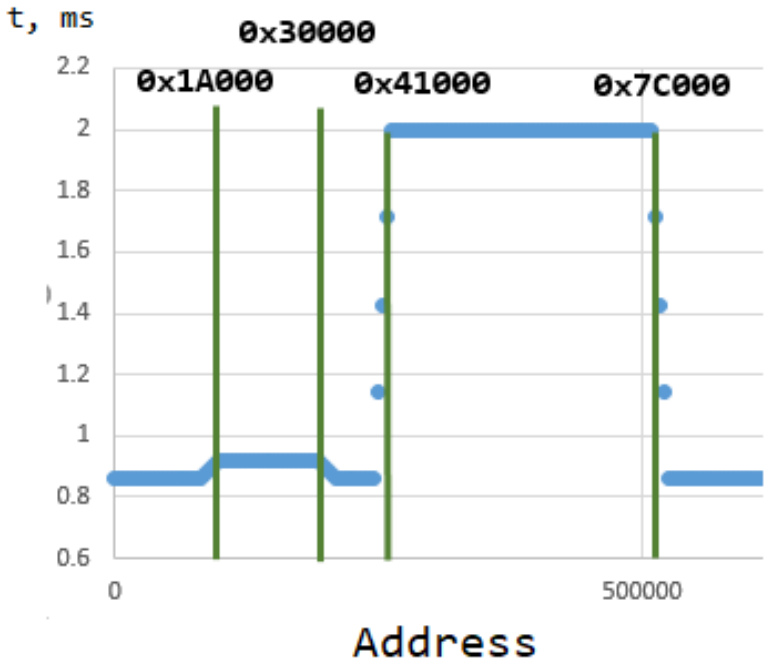
CRC32 command use case



CRC32 command use case

3.1. Memory Mapping

Module	Address (It is for Cluster CPU)
N-BROM	0x0000 0000---0x0000 BFFF
S-BROM	0x0000 0000---0x0000 FFFF
SRAM A1	0x0001 0000---0x0001 7FFF
SRAM A2	0x0004 4000---0x0005 3FFF
SRAM C	0x0001 8000---0x0003 FFFF
DE	0x0100 0000---0x013F FFFF
Core Sight Debug	0x0140 0000---0x0141 FFFF
CPU MBIST	0x0150 2000---0x0150 2FFF



CRC32 command use case

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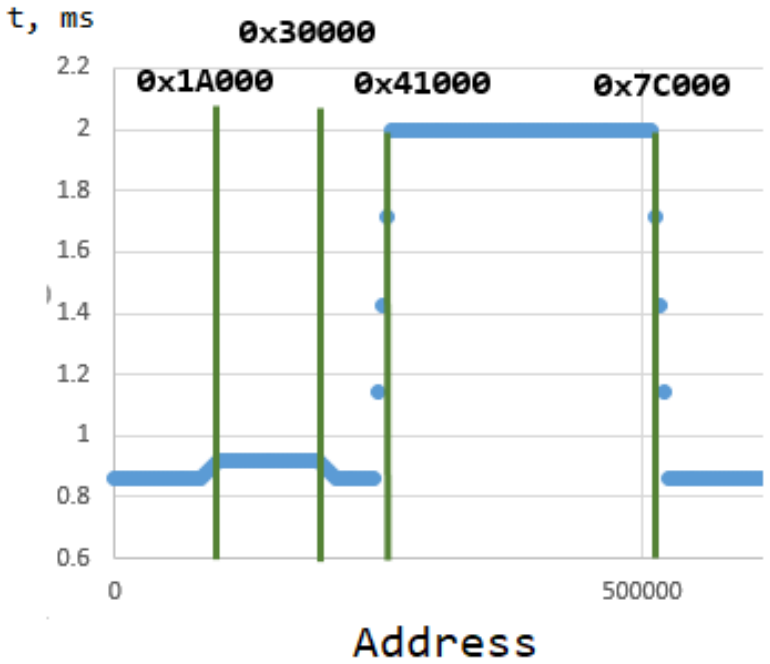
SRAM C	0x0001 8000---0x0003 FFFF
DE	0x0100 0000---0x013F FFFF
Core Sight Debug	0x0140 0000---0x0141 FFFF
CPU MBIST	0x0150 2000---0x0150 2FFF



What is at 0x00041000?

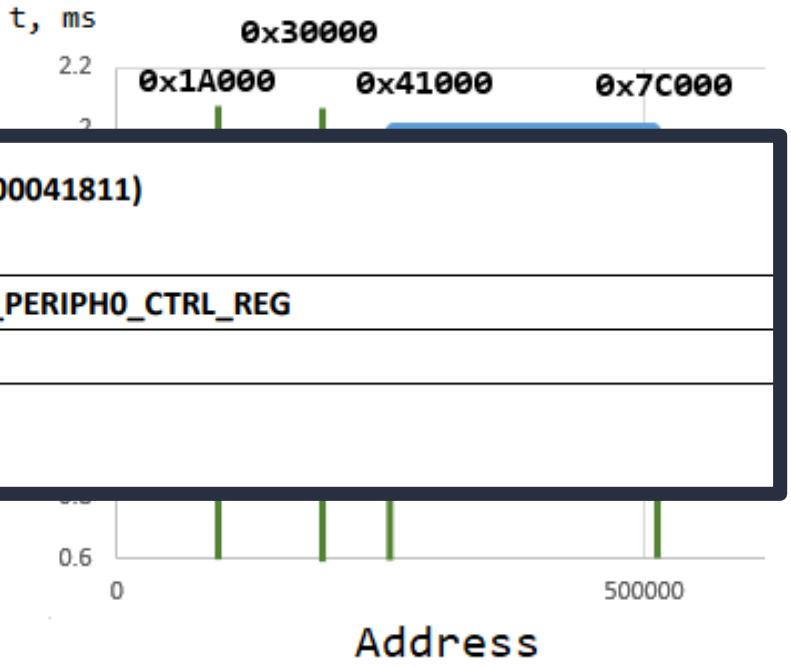
CRC32 command use case

3.1. Memory Mapping

Core Sight Debug	0x0140 0000---0x0141 FFFF
CPU MBIST	0x0150 2000---0x0150 2FFF

3.3.5.6. PLL_PERIPH0 Control Register (Default Value: 0x00041811)

Offset: 0x0028			Register Name: **PLL_PERIPH0_CTRL_REG**
Bit	R/W	Default/Hex	Description
31	R/W	0x0	PLL_ENABLE. 0: Disable



CRC32 command use case

- **CRC computation of 0x1000 bytes from different locations:**

Location	CRC command timing (len = 0x1000)
BROM	38 us
SRAM A1	38 us
SRAM A2	322 us
SRAM C	56 us
DDR	<29 us

Takeaways

- Coverage tracking for black box targets is possible
- Limited performance requires good corpus and syntax
- The approach can detect not only different SW execution paths, but also different HW

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Challenge your security